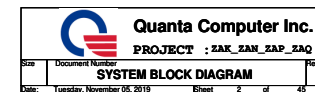


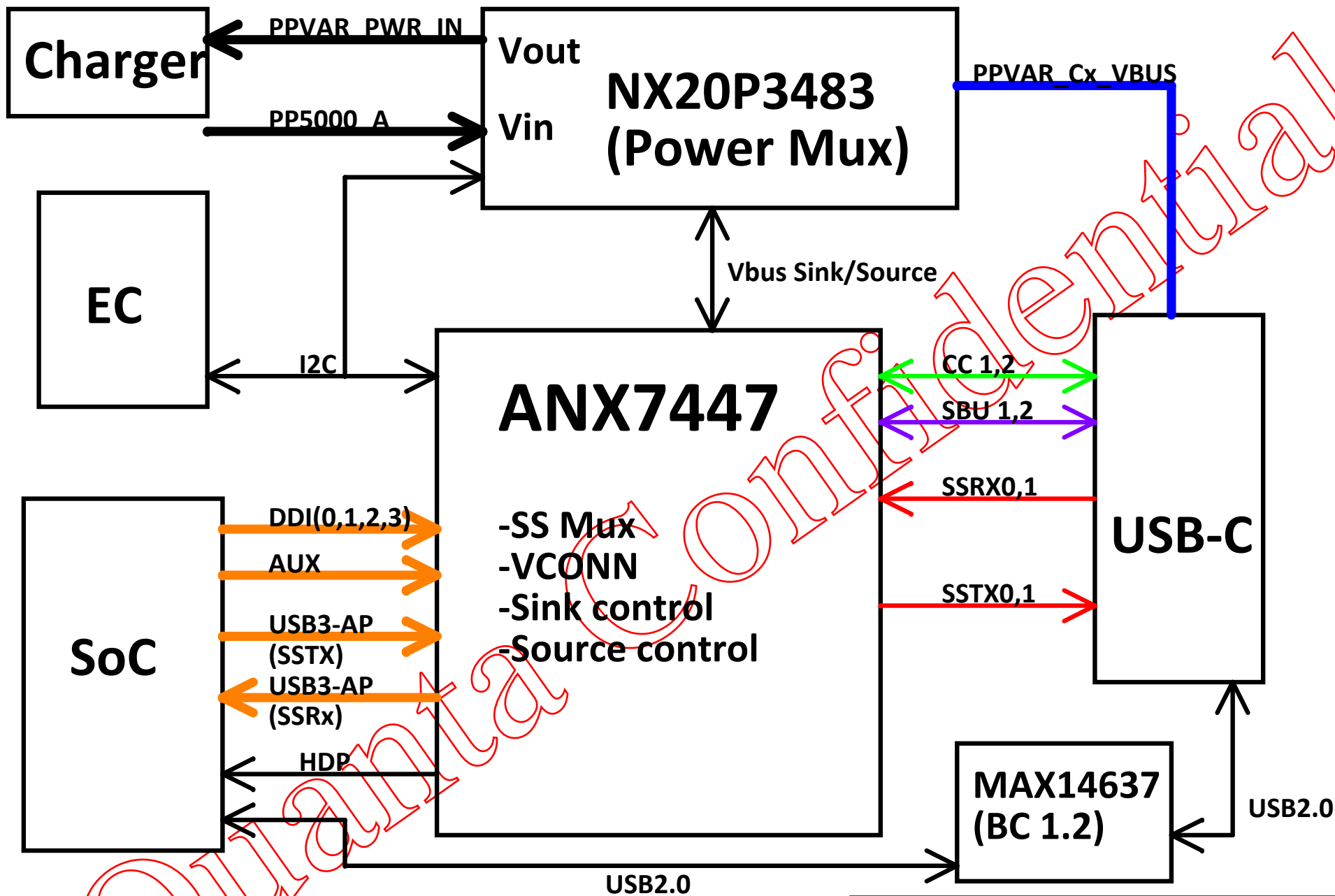
SCH: 650-01771-03-SCH
ASSY:650-01771-03
PCB: 651-01771-03

SHEET NO.	SHEET NAME
1	TABLE OF CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	USB TYPE-C BLOCK DIAGRAM
4	POWER TREE
5	I2C MAP
6	SOC DRAM I/F
7	SOC EDP/MIPI/DDI
8	SOC PCIE/USB/SATA
9	SOC AUDIO/EMMC/LPC/SPI
10	SOC I2C/CNVI/UART/SPI
11	SOC PMU/RTC/SVID/THERMAL/MISC
12	SOC JTAG/GPIO/ITP
13	SOC GROUND
14	SOC POWER
15	SOC DECOUPLING
16	MEMORY CH 00/01 LPDDR4
17	MEMORY CH 10/11 LPDDR4
18	EC-NUVOTON
19	SPI ROM
20	MIPI60 DEBUG HEADER
21	H1 SECURE MICROCONTROLLER
22	SERVO
23	eMMC/SD
24	AUDIO
25	KB, TP, PEN
26	LID: eDS, CAM, TOUCH, SENSOR
27	SENSOR: COMPASS, GYRO
28	WIFI/BT CONNECTOR
29	USB C TCPC/MUX
30	USB A CONNECTIONS (MLB)

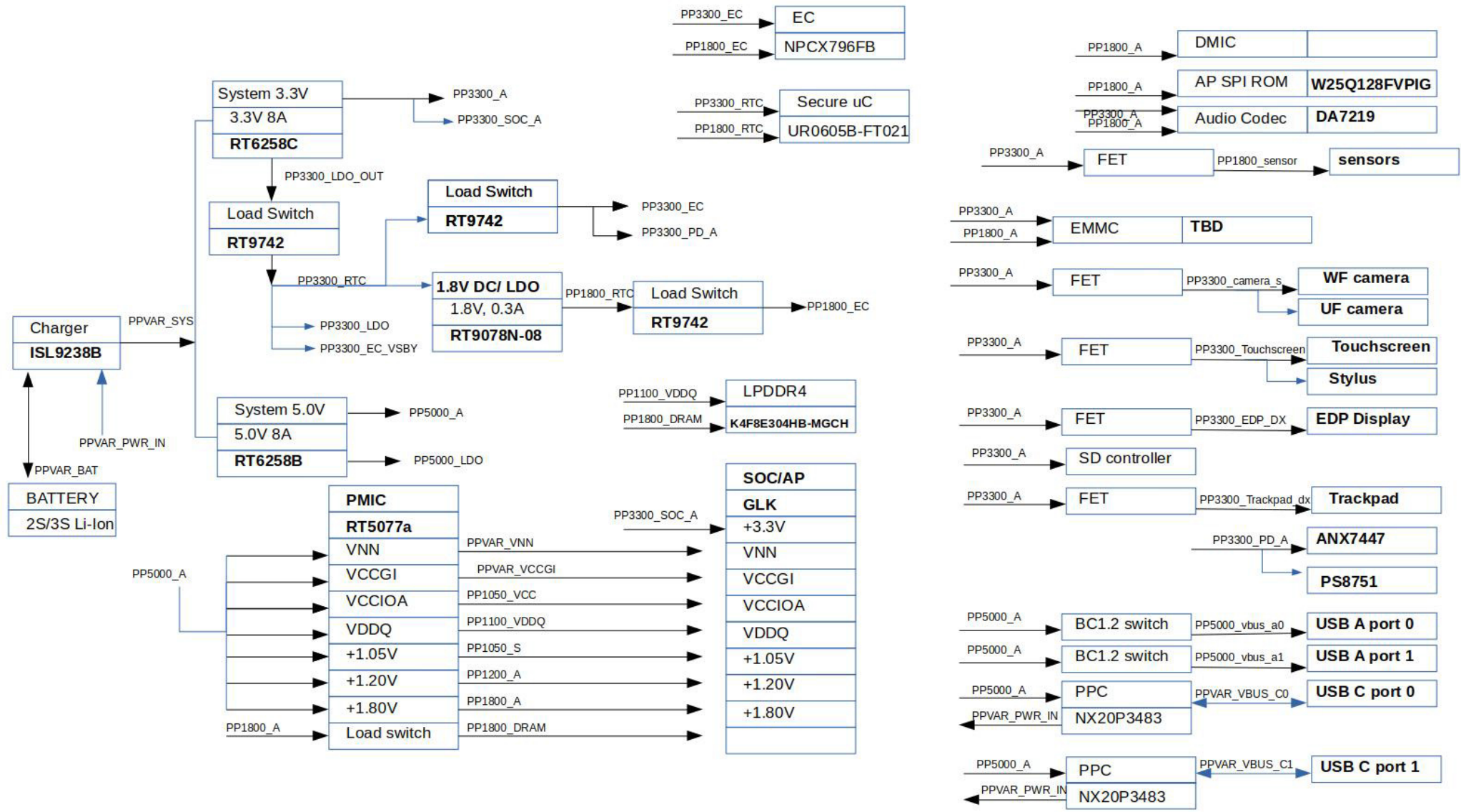
[illegible]

Apr, 24, 2018

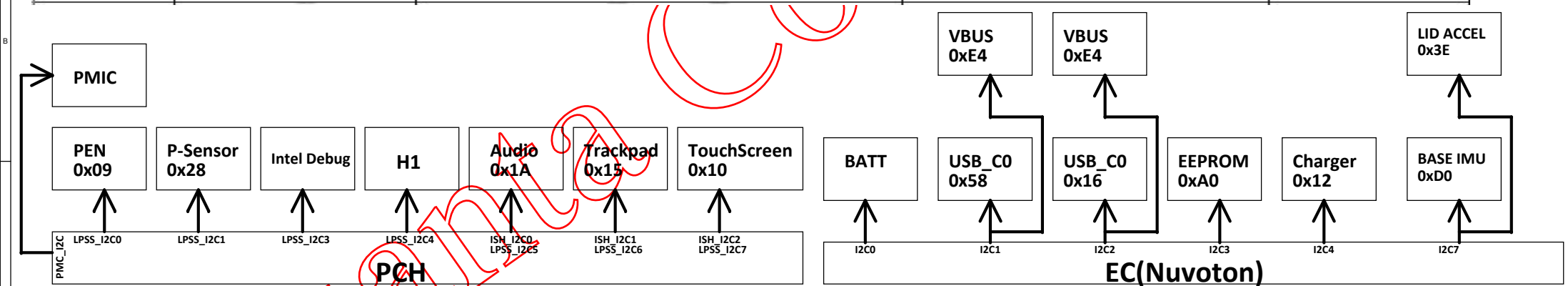


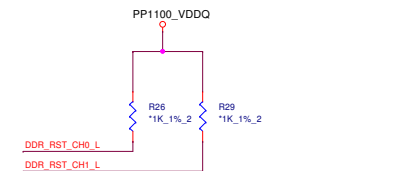
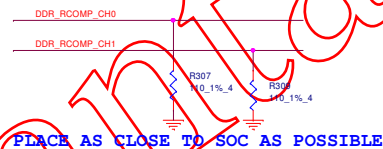


Power Tree

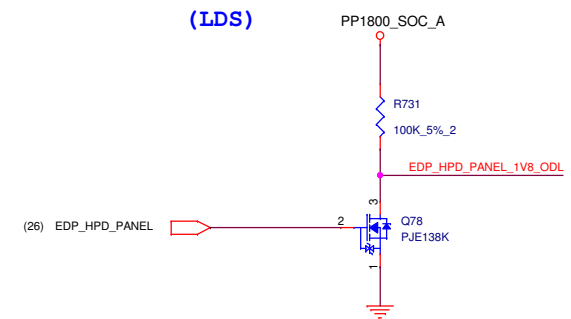
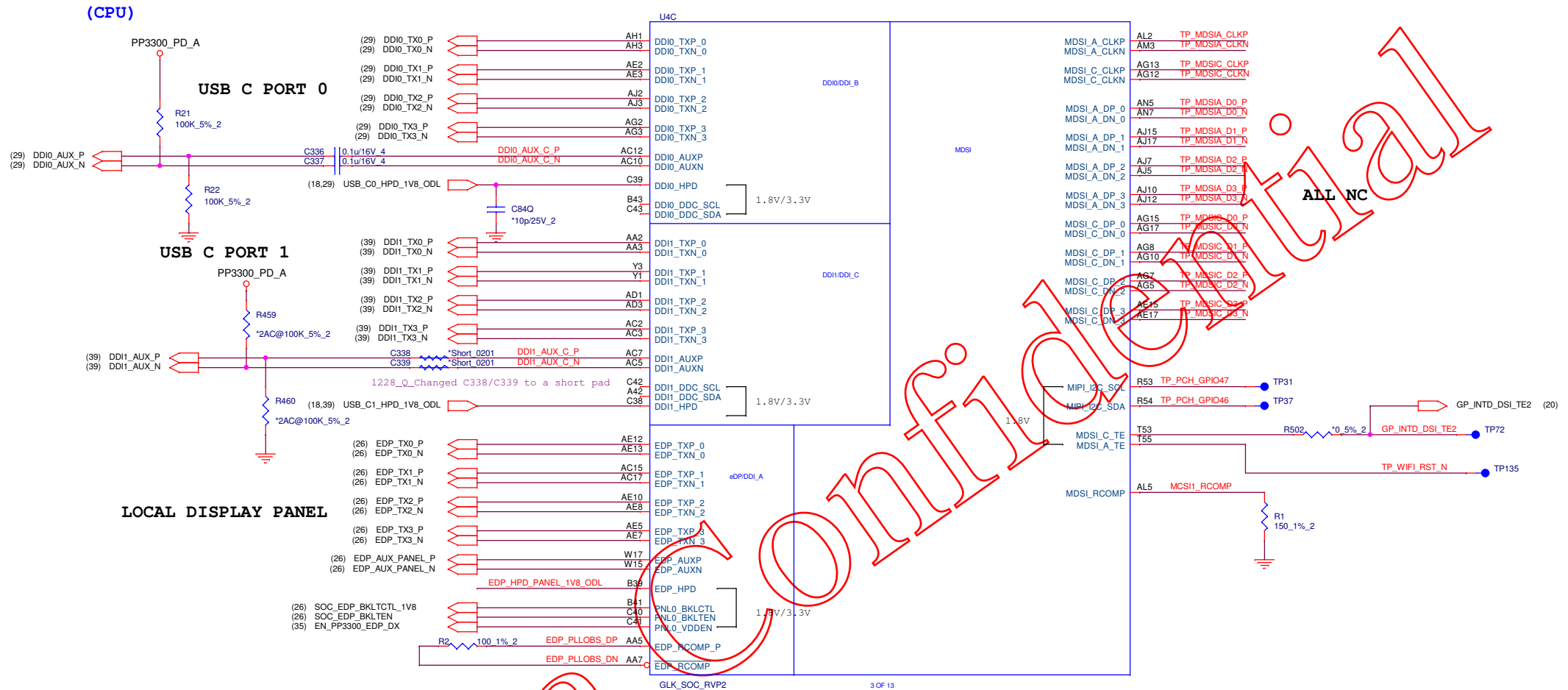


Master	Port	Net Name	Slave Device(S)	Speed
EC	I2C0 0	EC I2C BATTERY 3V3	BATTERY (TBD)	100KHZ
EC	I2C1 0	EC I2C USB C0 MUX	ANX7447, NX20P3483 <i>Check subboard</i>	100KHZ
EC	I2C2 0	EC I2C USB C1 MUX		100KHZ
EC	I2C3 0	EC I2C EEPROM SCL	M34E02	100KHZ
EC	I2C4 1	EC I2C CHARGER 3V3	ISL9238B	100KHZ
EC	I2C5 0	-		
EC	I2C7 0	EC I2C SENSOR U	LSM6DS3TR, LIS2MDLTR	400KHZ
AP	LPSS I2C0	PCH I2C PEN	STYLUS (TBD)	400KHZ
AP	LPSS I2C1	PCH I2C P SENSOR	TBD	100KHZ
AP	LPSS I2C2	-		
AP	LPSS I2C3	DBG PCH I2C	TBD	TBD
AP	LPSS I2C4	PCH I2C H1	H1 (not used)	100KHZ
AP	LPSS I2C5	PCH I2C AUDIO	DA7219	100KHZ
AP	LPSS I2C6	PCH I2C TRACKPAD	TRACKPAD (TBD)	100KHZ
AP	LPSS I2C7	PCH I2C TOUCHSCREEN	TOUCHSCREEN (TBD)	100KHZ
AP	PMC I2C	PCH PMIC I2C	RT5077A	100KHZ



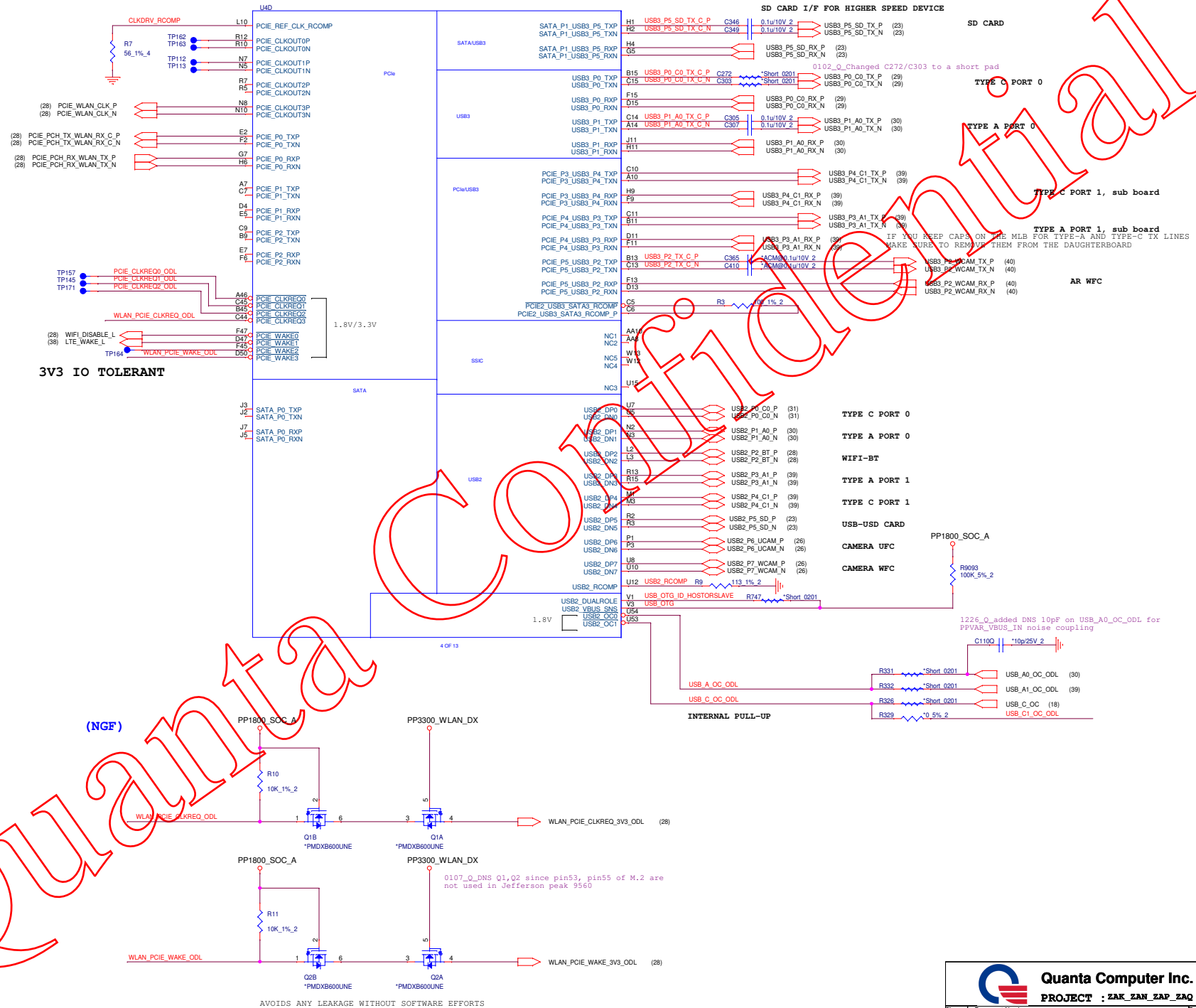


Gemini lake (DISPLAY, eDP)



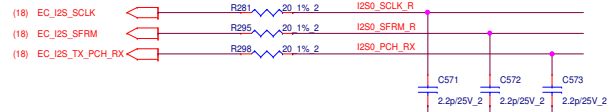
Gemini lake (SATA , ODD, CLK ,USB,PCIE)

(CPU)

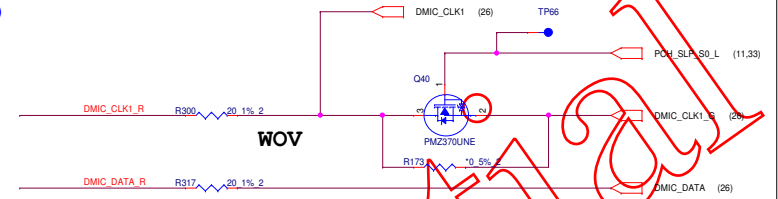


Gemini lake (EMMC/LPC/I2C/GPIO/HDA)

(CPU)



(MIC)



(CPU)

TO-EC

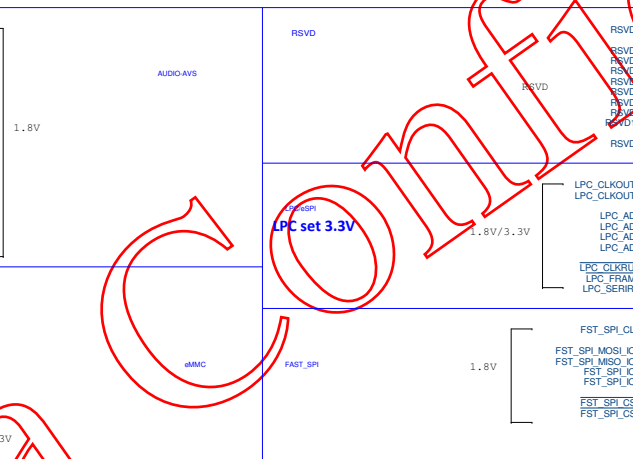
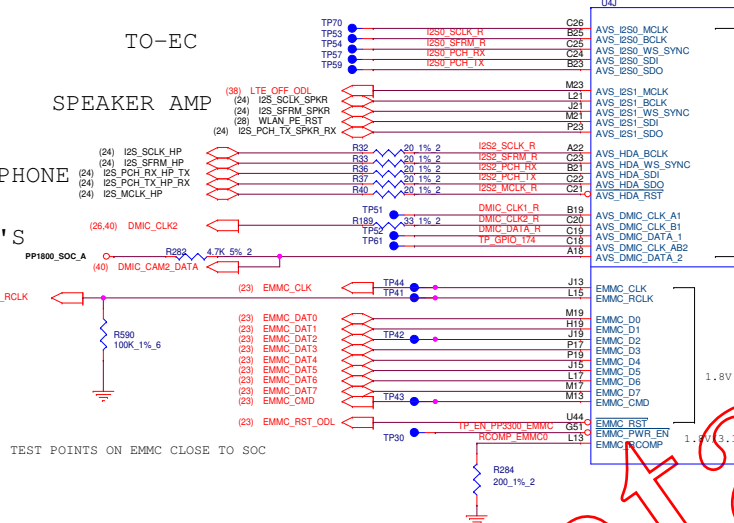
SPEAKER AMP

HEADPHONE

DMIC'S

PP1800_SOC_A

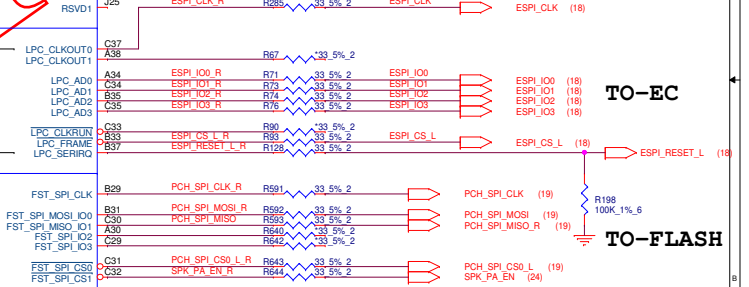
TEST POINTS ON EMMC CLOSE TO SOC



native SD card support dropped

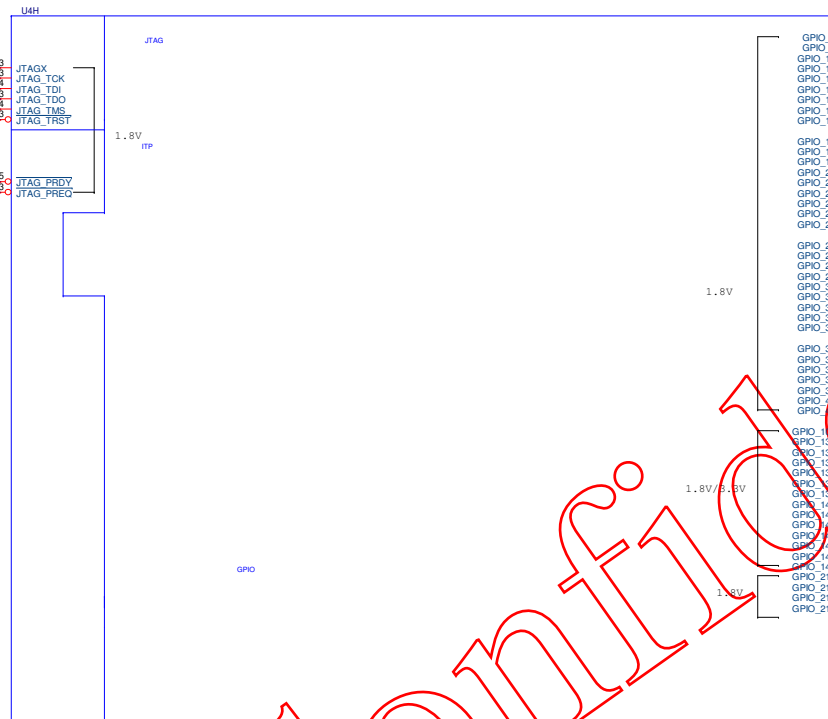
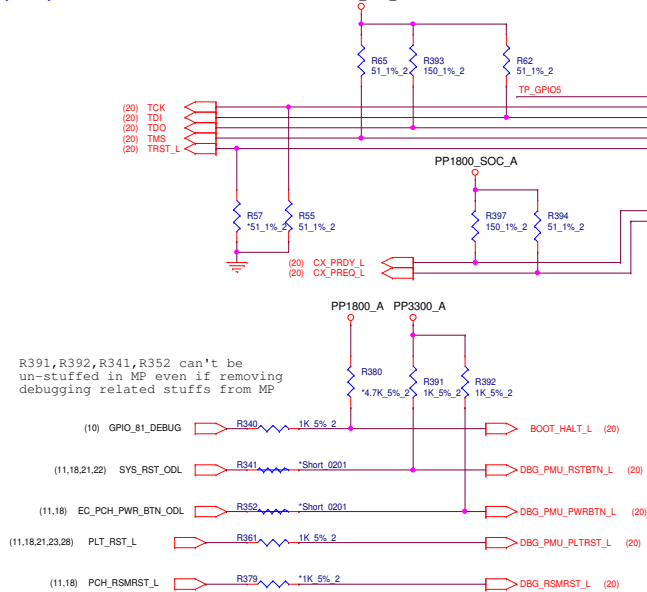
TO-EC

TO-FLASH

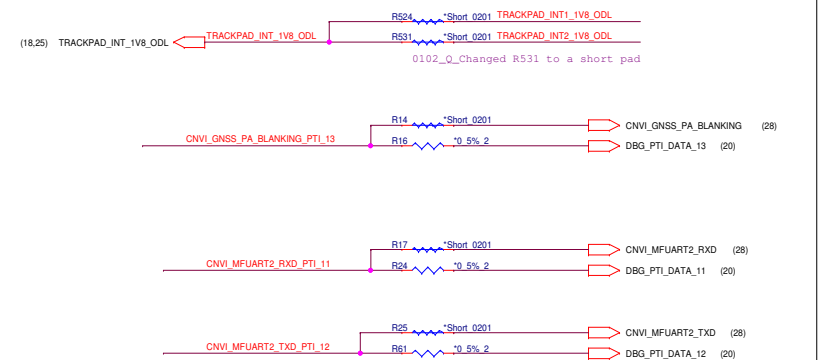


(CPU)

PP1800_SOC_A



1226_Q made R289 stuffed for no matter internal PU is available or not



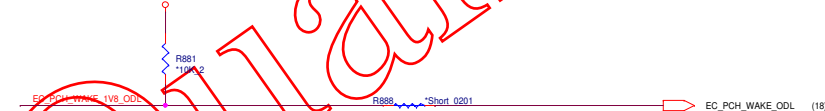
(PMC)

PP1800_SOC_A



(CPU)

PP1800_SOC_A



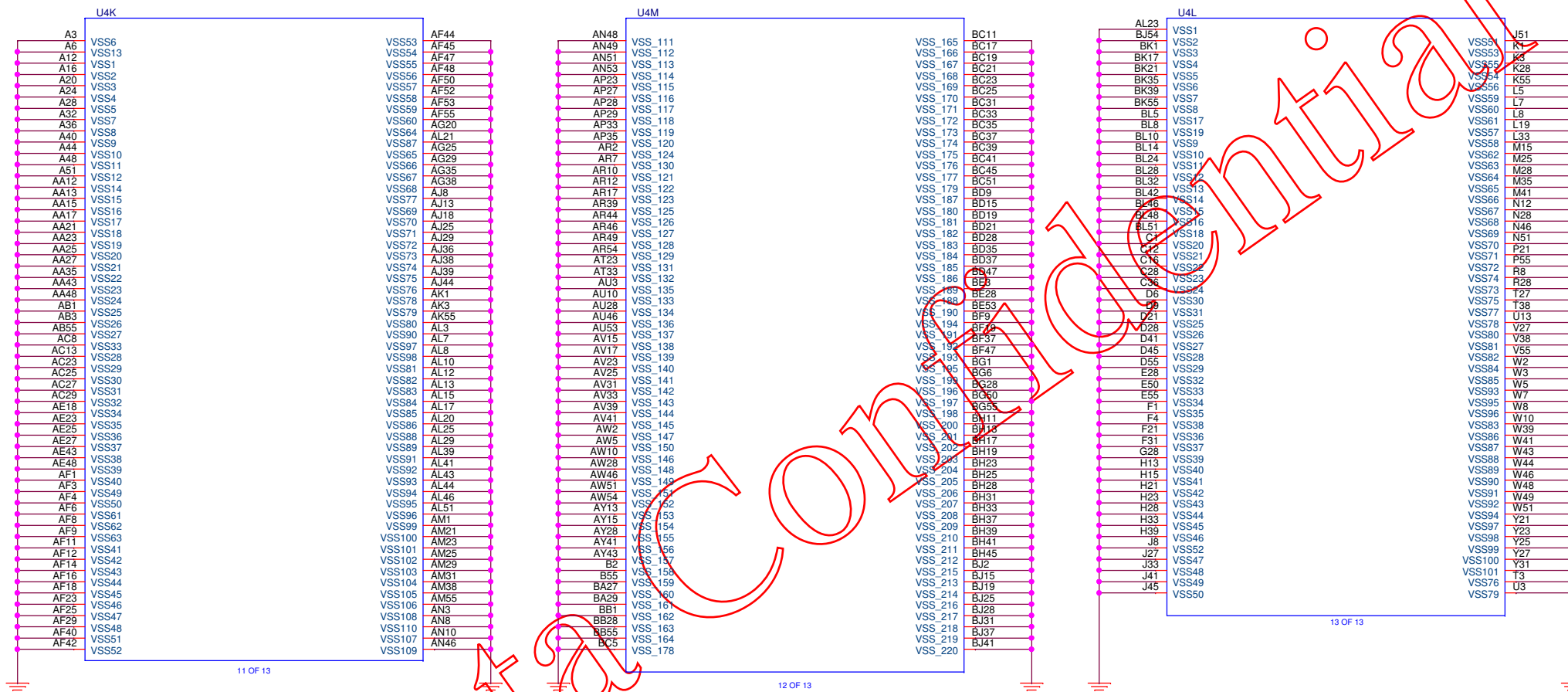
R380 is reserved for strapping high (GPIO_81)

R877 is for strapping low to not allow eMMC as a boot source (GPIO_27)

No external PU/PD on GPIO_28, using internal PD for allowing SPI as a boot source

(CPU)

GLK ULT (GND)

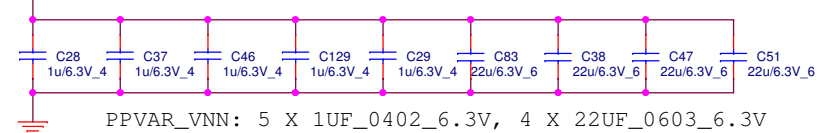


Gemini (POWER)

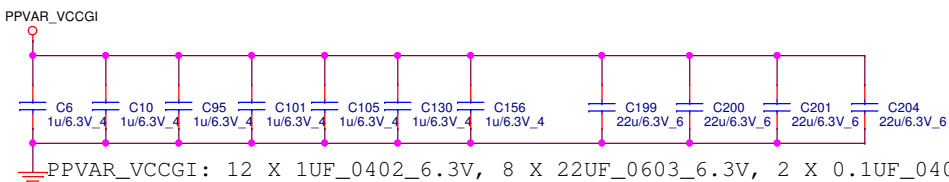


03/20 Change FF to SHORT92X32

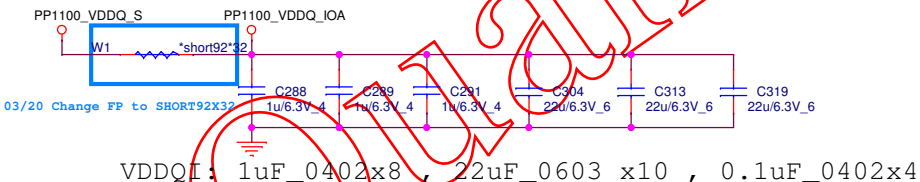
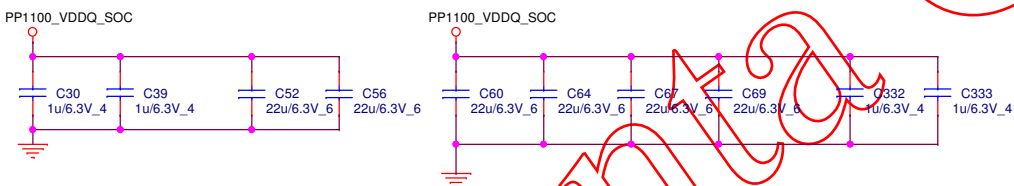
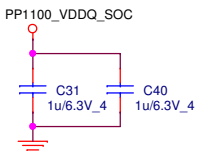
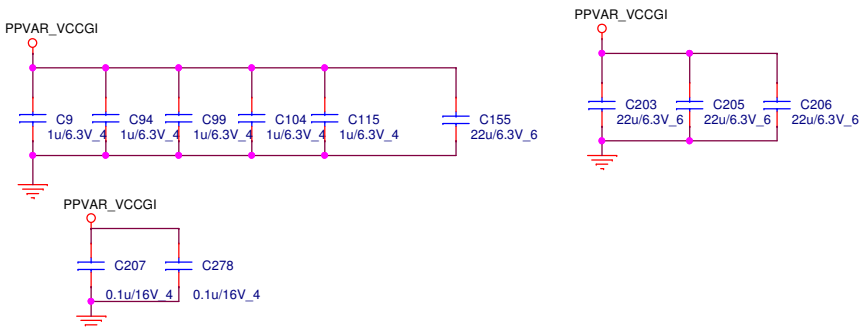
(CPU)
PPVAR_VNN
DECOUPLING VALUES AND NUMBER BASED ON THE REFERENCE DOC



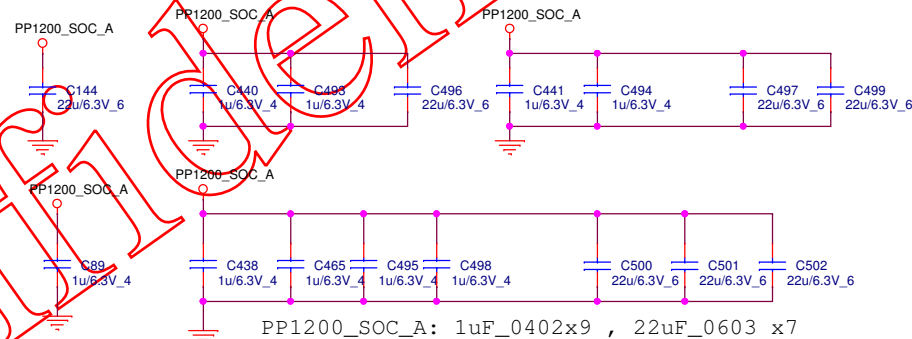
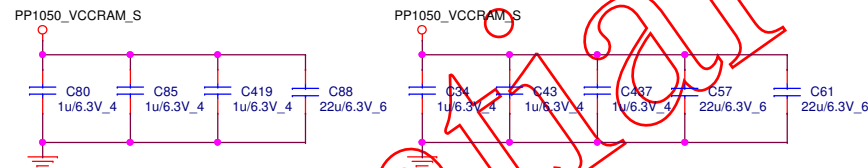
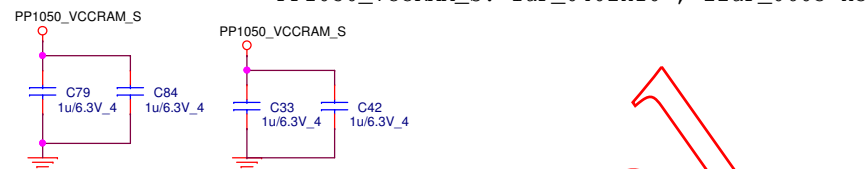
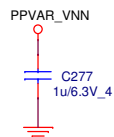
PPVAR_VNN: 5 X 1UF_0402_6.3V, 4 X 22UF_0603_6.3V



PPVAR_VCCGI: 12 X 1UF_0402_6.3V, 8 X 22UF_0603_6.3V, 2 X 0.1UF_0402_16V

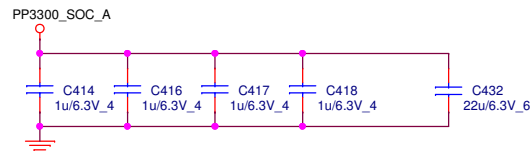
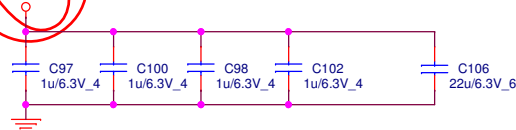


VDDQI: 1uF_0402x8, 22uF_0603 x10, 0.1uF_0402x4

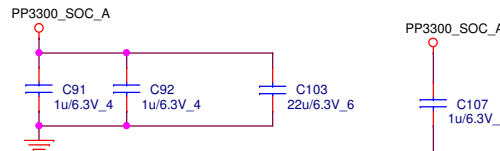


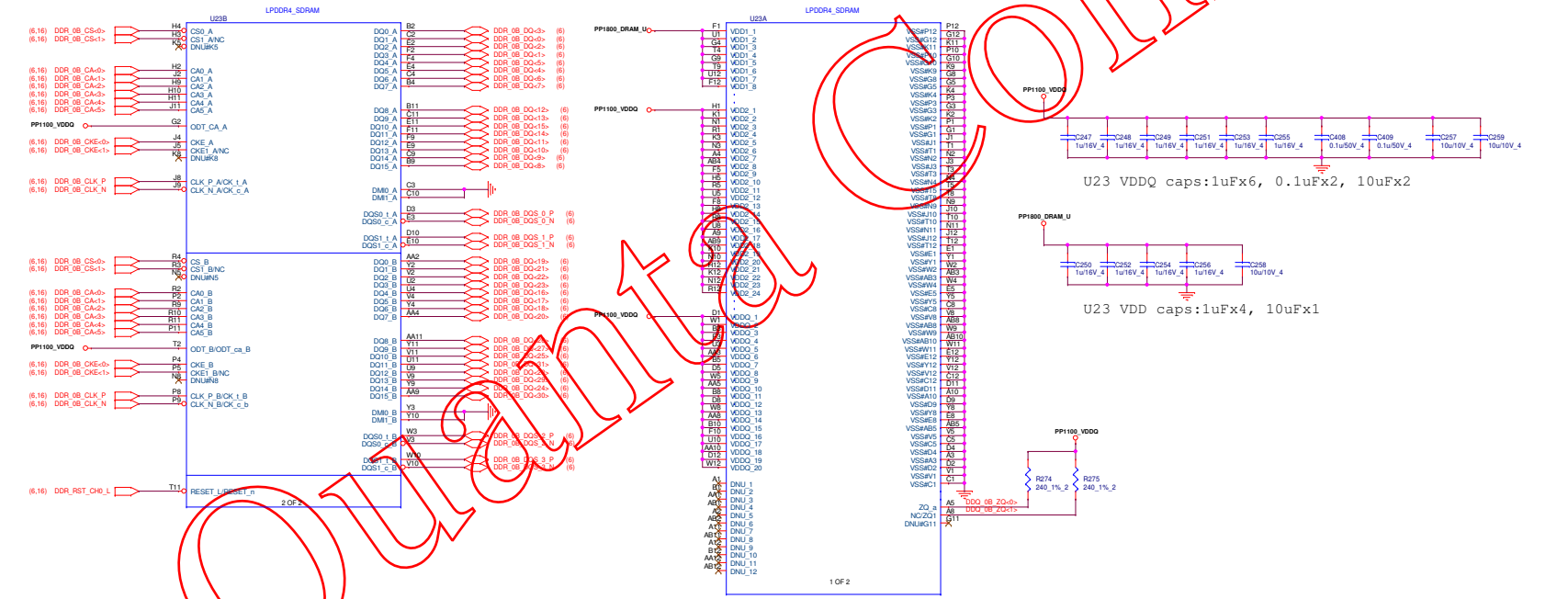
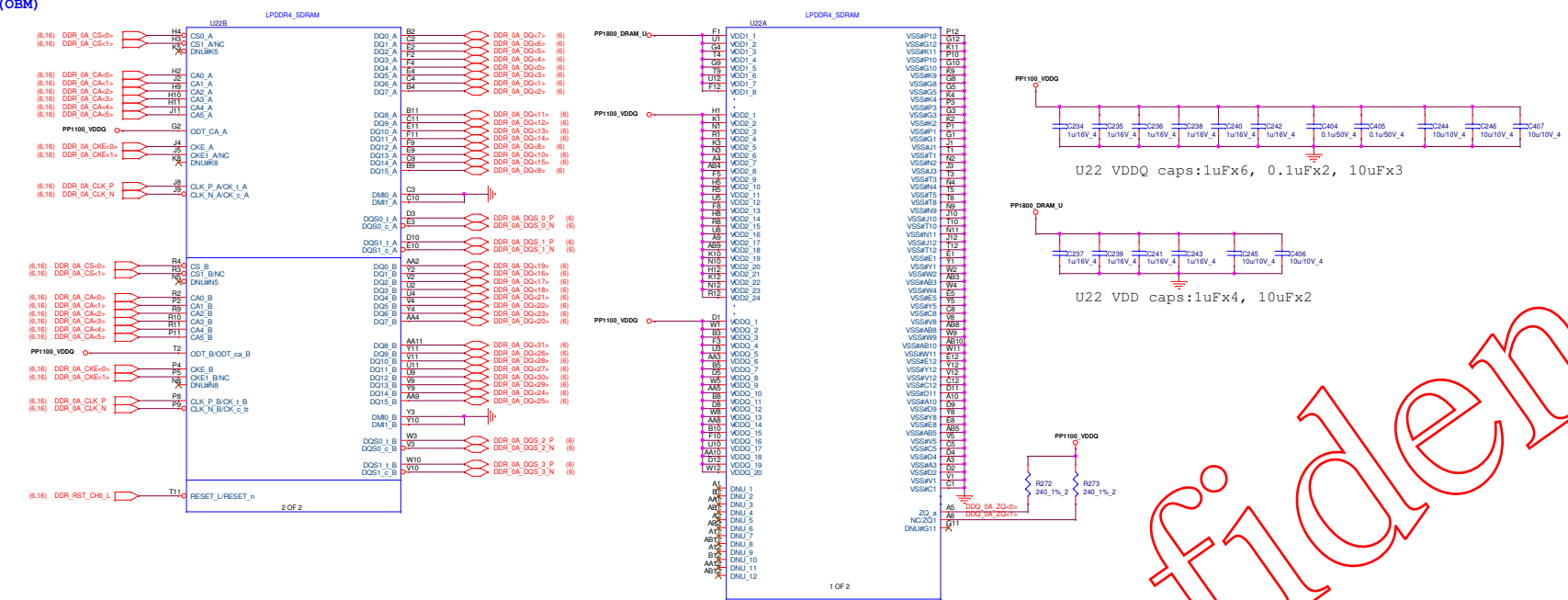
PP1200_SOC_A: 1uF_0402x9, 22uF_0603 x7

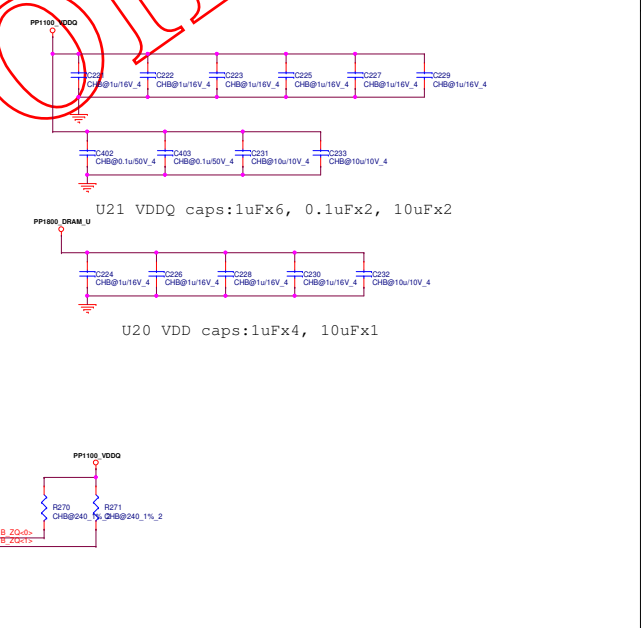
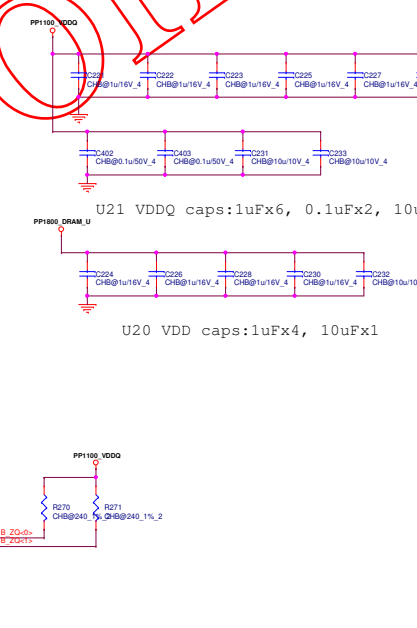
PP1800_SOC_A: 1uF_0402x4, 22uF_0603 x1

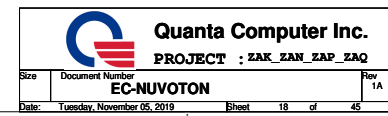


PP3300_SOC_A: 1uF_0402x8, 22uF_0603 x2

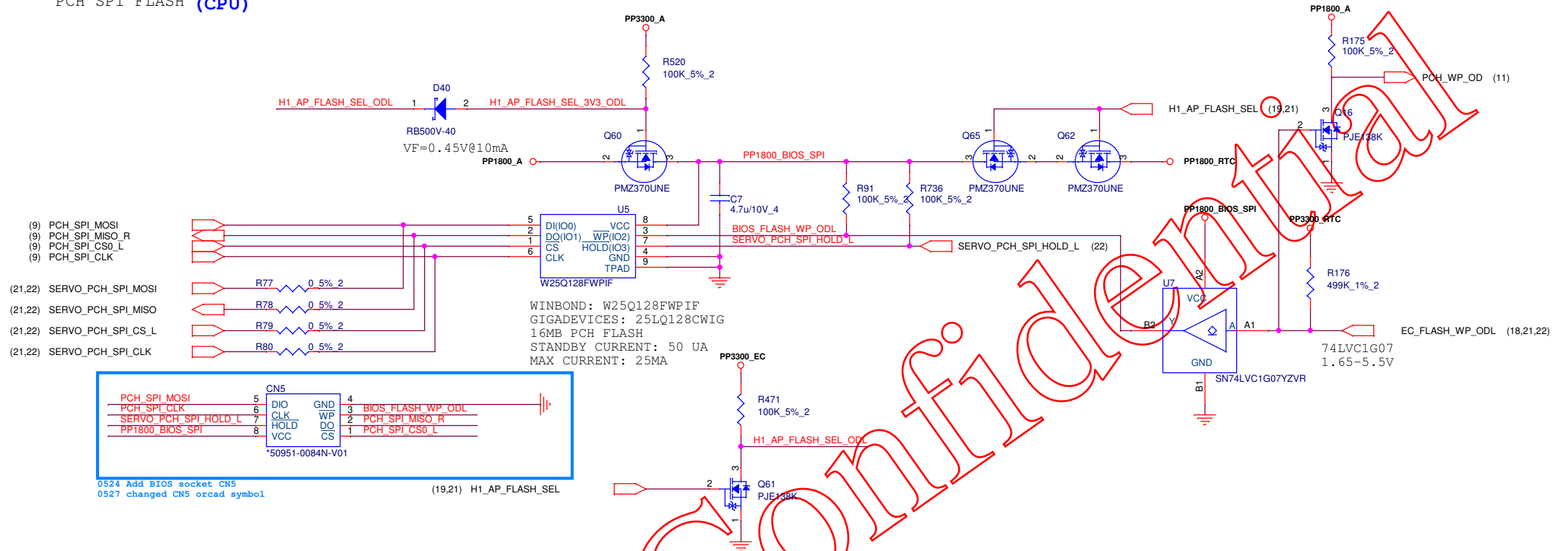




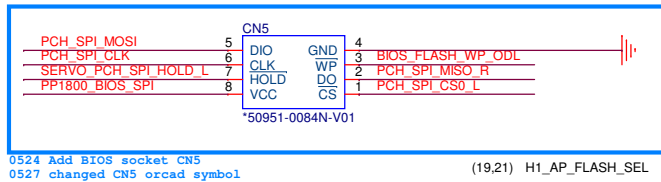




PCH SPI FLASH (CPU)

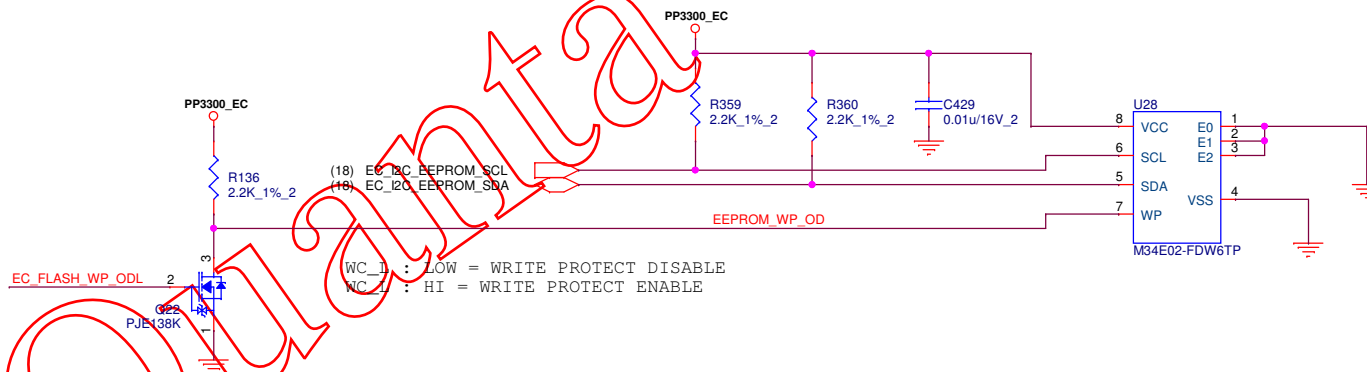


WINBOND: W25Q128FWPIF
GIGADEVICES: 25LQ128CWIG
16MB PCH FLASH
STANDBY CURRENT: 50 UA
MAX CURRENT: 25MA

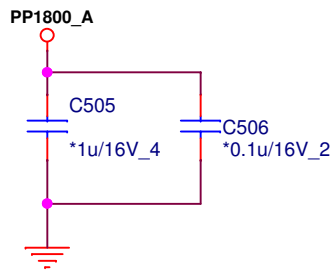


(KBC)

SKU EEPROM



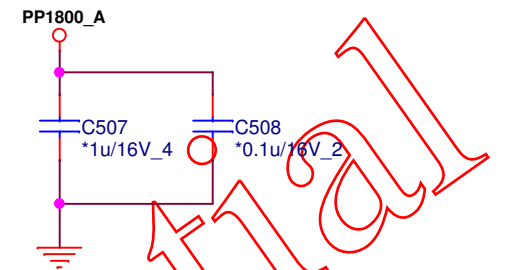
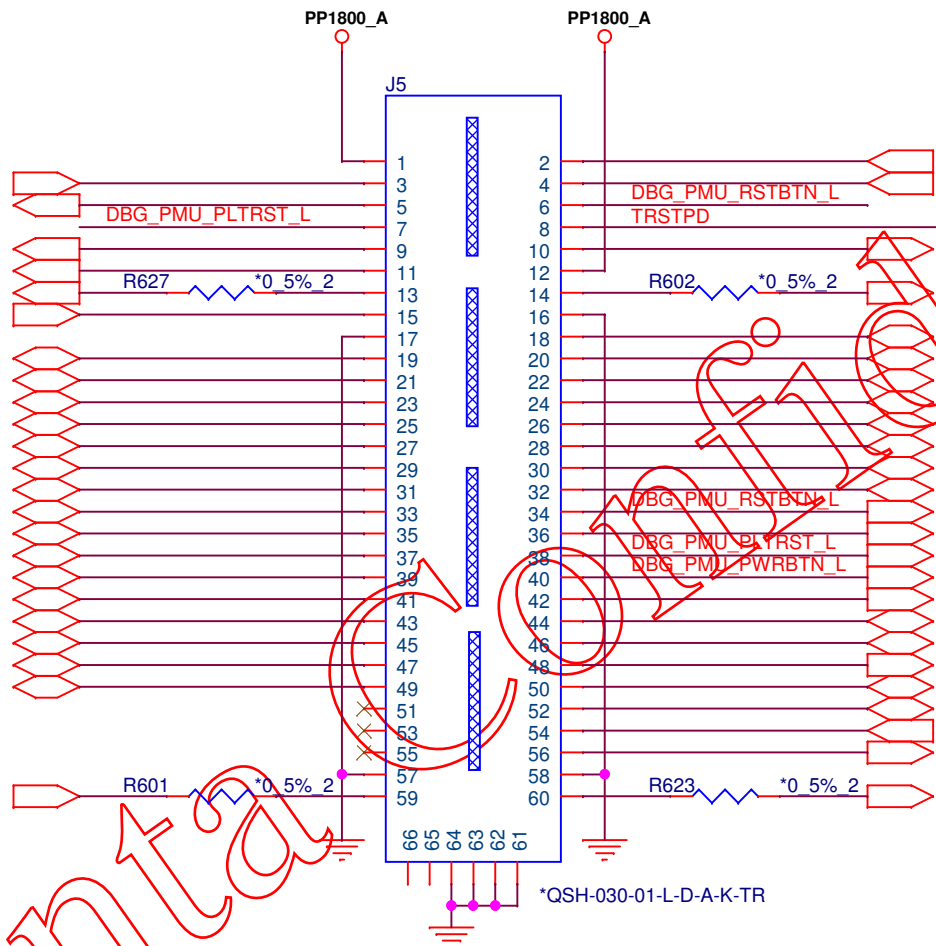
(INT)



LAYOUT NOTE: PLACING THE SERIAL R'S WITHIN 1 " OF THE DEBUG CONNECTOR

- (12) TCK
- (12) TDI
- (12) TRST_L
- (12) CX_PRDY_L
- (12) DBG_PTI_CLK0
- (7) GP_INTD_DSI_TE2
- (12) DBG_PTI_DATA_0
- (12) DBG_PTI_DATA_1
- (12) DBG_PTI_DATA_2
- (12) DBG_PTI_DATA_3
- (12) DBG_PTI_DATA_4
- (12) DBG_PTI_DATA_5
- (12) DBG_PTI_DATA_6
- (12) DBG_PTI_DATA_7
- (12) DBG_PTI_DATA_8
- (12) DBG_PTI_DATA_9
- (12) DBG_PTI_DATA_10
- (12) DBG_PTI_DATA_11
- (12) DBG_PTI_DATA_12
- (12) DBG_PTI_DATA_13
- (12) DBG_PTI_DATA_14
- (12) DBG_PTI_DATA_15

(12) DBG_PTI_CLK1



TMS (12)
TDO (12)

CX_FREQ_L (12)

DBG_PTI_CLK2 (12)

DBG_PTI_DATA_16 (12)

DBG_PTI_DATA_17 (12)

DBG_PTI_DATA_18 (12)

DBG_PTI_DATA_19 (12)

DBG_PTI_DATA_20 (12)

DBG_PTI_DATA_21 (12)

DBG_PTI_DATA_22 (12)

DBG_PTI_DATA_23 (12)

DBG_PMI_RSTBTN_L (12)

BOOT_HALT_L (12)

DBG_PMI_PLTRST_L (12)

DBG_PMI_PWRBTN_L (12)

DBG_RSMRST_L (12)

DCI_DATA_PTITRACE3_0 (12)

DBG_PTI_DATA_TRACE3_1 (12)

DBG_PCH_I2C_SCL (10)

DBG_PCH_I2C_SDA (10)

DBG_PTI_DATA_TRACE3_2 (12)

PCHTX_MIP160RX_UART (10)

PCHRX_MIP160TX_UART (10)

DCI_CLK_PTICLK3 (12)

R199
*10K_1%_2

DBG_PMI_RSTBTN_L

C93
*0.01u/16V_2

DBG_PMI_PWRBTN_L

C78
*0.01u/16V_2

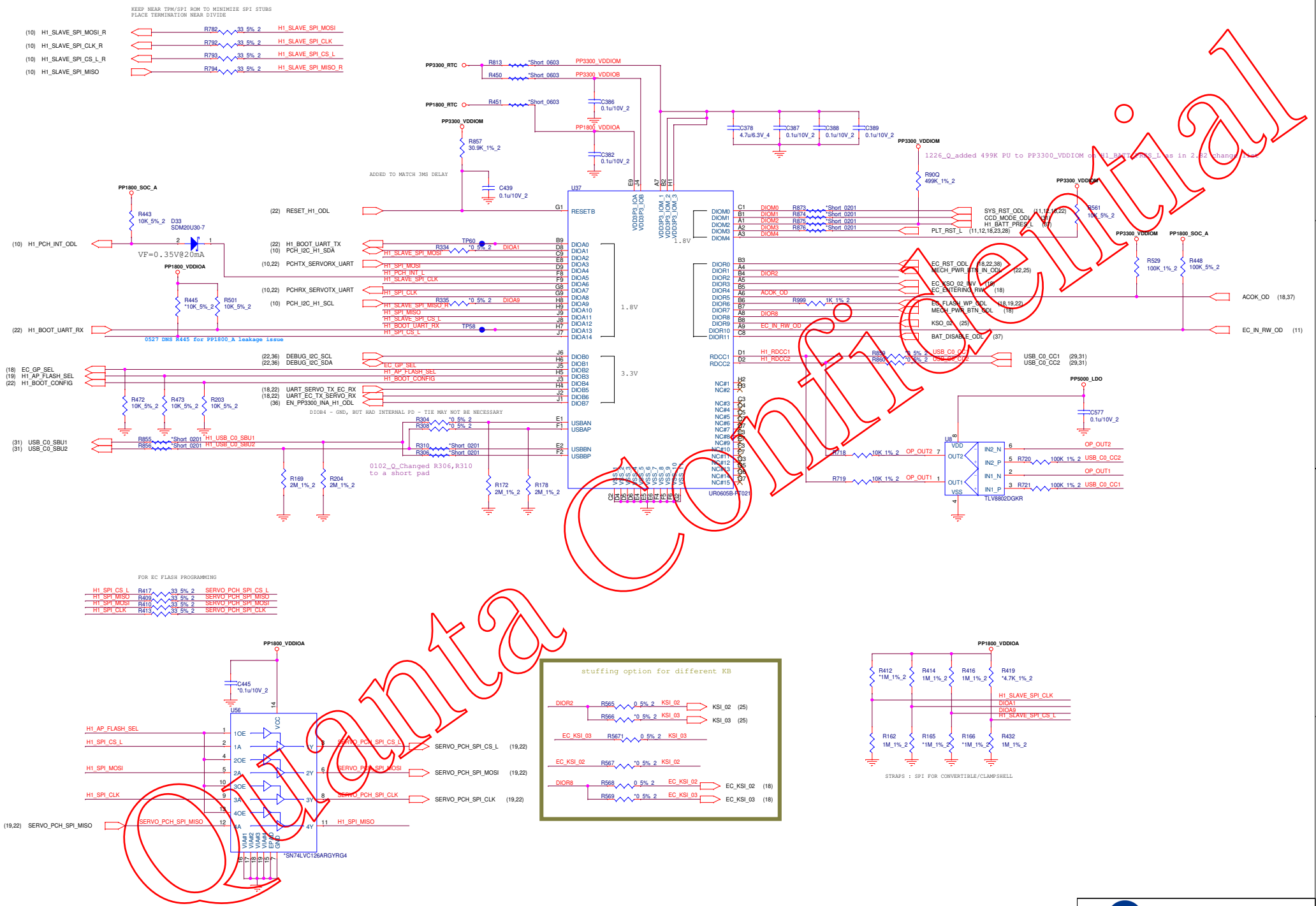


Quanta Computer Inc.

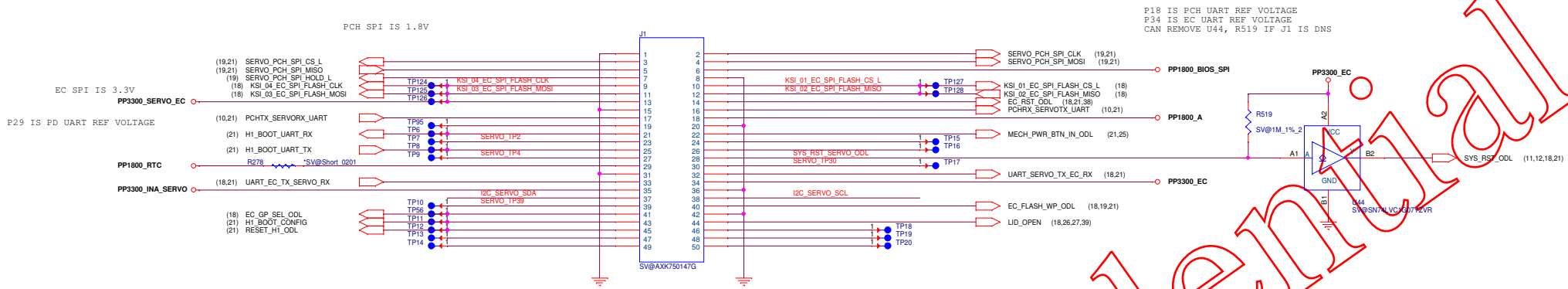
PROJECT : ZAK_ZAN_ZAP_ZAQ

Size	Document Number	Rev
	MIPI60 DEBUG HEADER	1A
Date:	Tuesday, November 05, 2019	Sheet 20 of 45

(H1C)



(GOG)

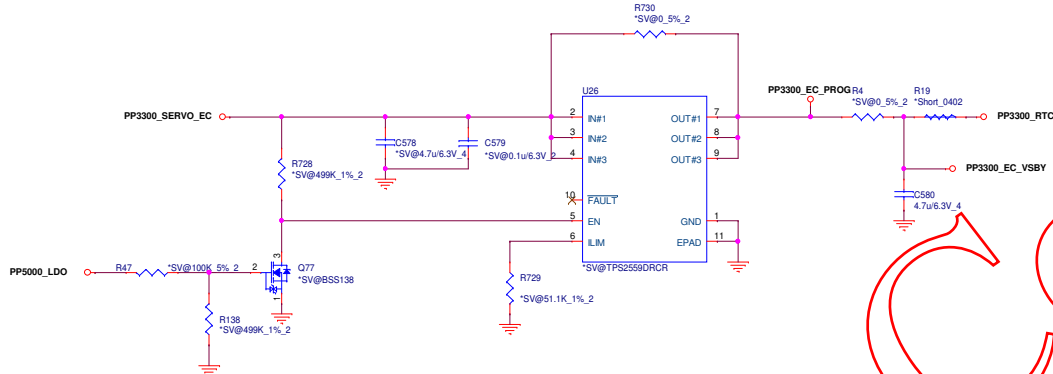


SERVO HEADER

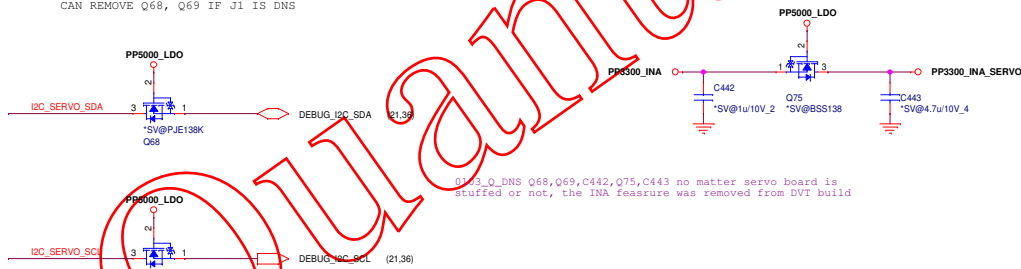
(H1C)

POWER FOR FLASHING EC THROUGH SERVO

CAN REMOVE U44, U26, Q77, C578, C579, R128, R47, R138 R519 IF J1 IS DNS

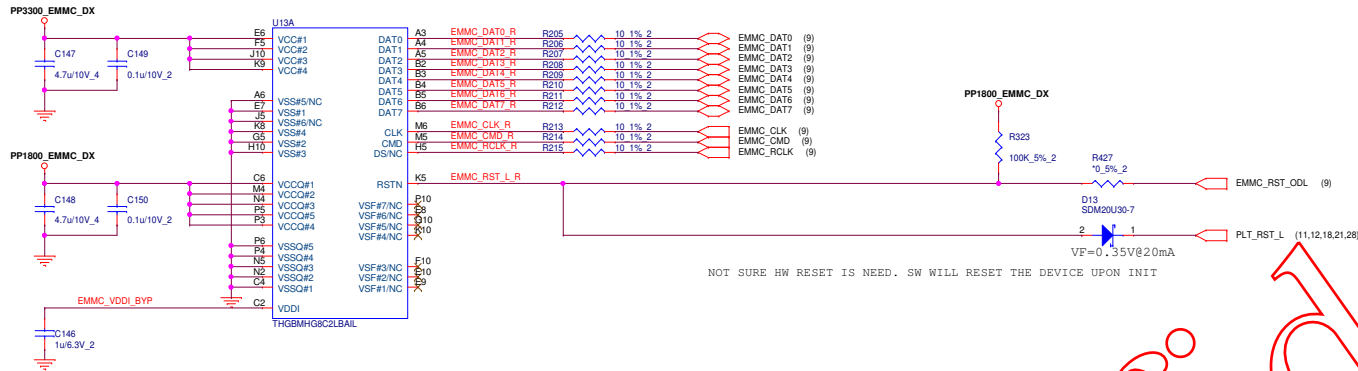


CAN REMOVE Q68, Q69 IF J1 IS DNS



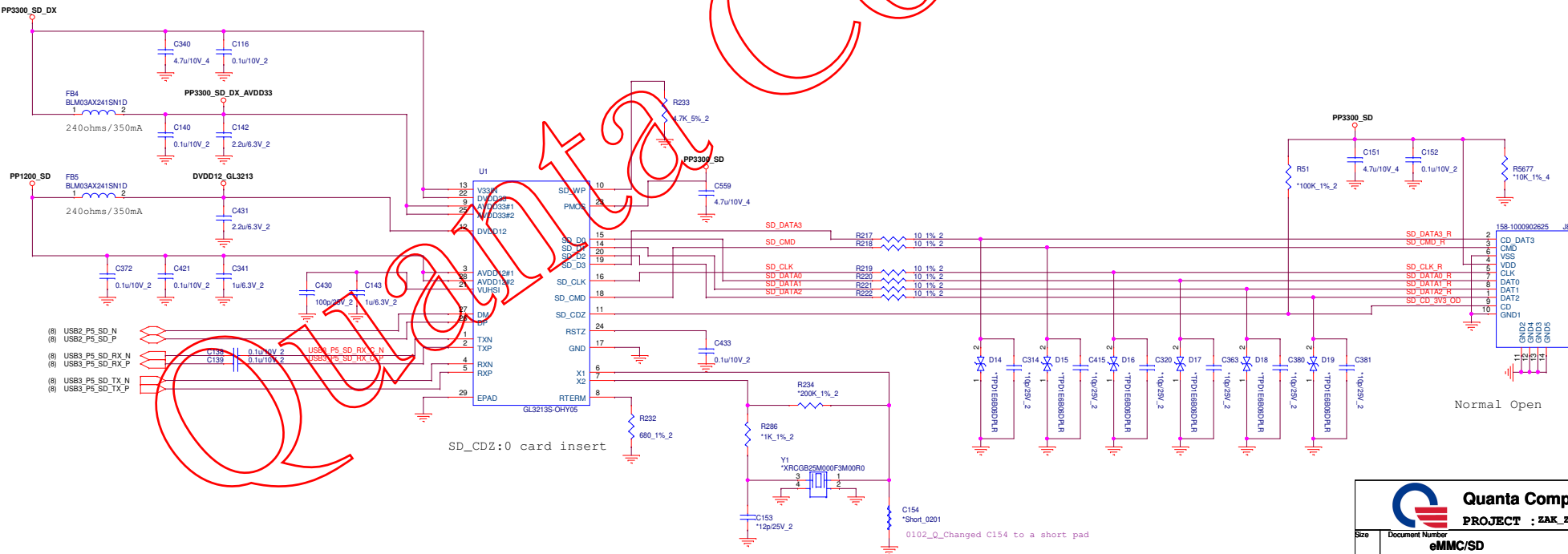
Q68,Q69,Q75,C442,Q75,C443 no matter servo board is stuffed or not, the INA feature was removed from DVT build

(MMC) 32 GB EMMC STORAGE
150 uA SLEEP CURRENT



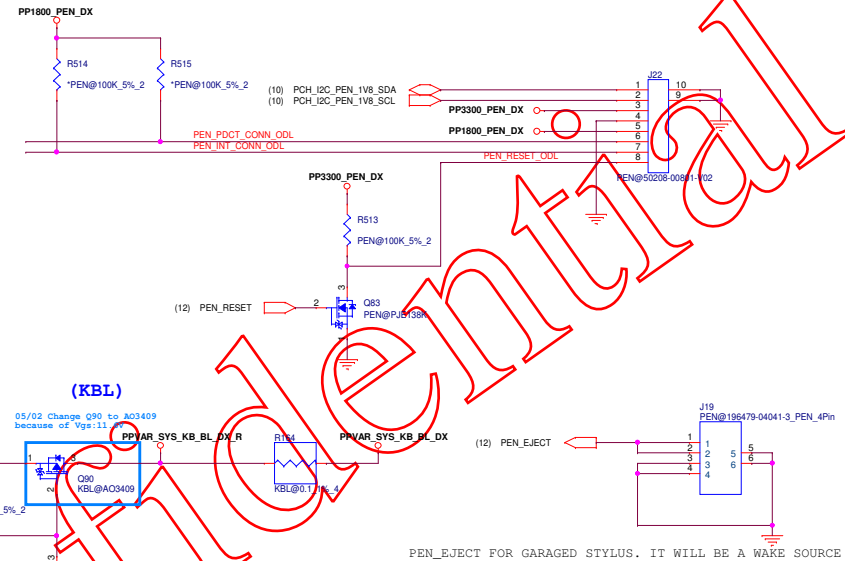
U13B			
A1	NC#A1	NC#H2	H2
A2	NC#A2	NC#H3	H3
A7	RFU#A7/NC	NC#H12	H12
A8	NC#A8	NC#H13	H13
A9	NC#A9	NC#H14	H14
A10	NC#A10	NC#H1	H1
A11	NC#A11	NC#H2	H2
A12	NC#A12	NC#H3	H3
A13	NC#A13	NC#H12	H12
B1	NC#B1	NC#H13	H13
B7	NC#B7	NC#H14	H14
B8	NC#B8	NC#H1	H1
B9	NC#B9	NC#H2	H2
B10	NC#B10	NC#H3	H3
B11	NC#B11	RFU#B11/NC	
B12	NC#B12	RFU#B12/NC	
B13	NC#B13	NC#H12	H12
B14	NC#B14	NC#H13	H13
C1	NC#C1	NC#H14	H14
C3	NC#C3	NC#H1	H1
C5	NC#C5	NC#H2	H2
C7	NC#C7	NC#H3	H3
C8	NC#C8	NC#H12	H12
C9	NC#C9	NC#H13	H13
C10	NC#C10	NC#H14	H14
C11	NC#C11	NC#H1	H1
C12	NC#C12	NC#H2	H2
C13	NC#C13	NC#H3	H3
C14	NC#C14	NC#H12	H12
D1	NC#D1	NC#H13	H13
D2	NC#D2	NC#H14	H14
D3	NC#D3	NC#H1	H1
D4	NC#D4	NC#H2	H2
D12	NC#D12	NC#H3	H3
D13	NC#D13	NC#H12	H12
D14	NC#D14	NC#H13	H13
E1	NC#E1	NC#H14	H14
E2	NC#E2	NC#H1	H1
E3	NC#E3	NC#H2	H2
E4	NC#E4	NC#H3	H3
E13	NC#E13	NC#H12	H12
E14	NC#E14	NC#H13	H13
F1	NC#F1	NC#H14	H14
F2	NC#F2	NC#H1	H1
F3	NC#F3	NC#H2	H2
F13	NC#F13	NC#H3	H3
F14	NC#F14	NC#H12	H12
G1	NC#G1	NC#H13	H13
G2	NC#G2	NC#H14	H14
G3	NC#G3	NC#H1	H1
G12	RFU#G12/NC	NC#H2	H2
G13	NC#G13	NC#H3	H3
G14	NC#G14	NC#H12	H12
H1	NC#H1	NC#H13	H13

(CRD) MICRO SD CARD



PEN/STYLUS CONNECTOR

TOUCHSCREEN AND PEN/STYLUS POWER TOGETHER
(PEN)



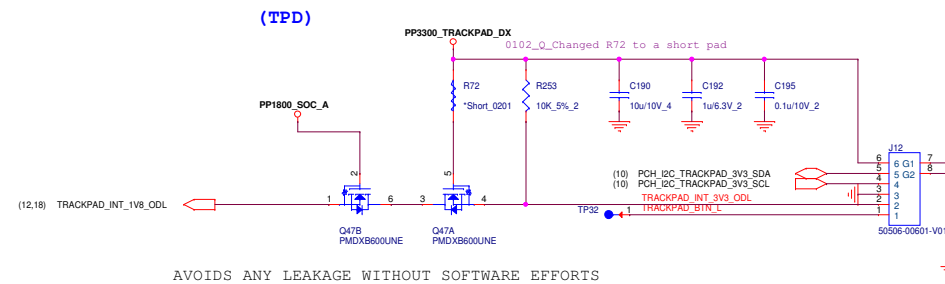
PEN_EJECT FOR GARAGED STYLUS. IT WILL BE A WAKE SOURCE

KEYBOARD

[illegible]

TRACKPAD CONNECTOR

CM TO CHOOSE CONNECTOR




AVOIDS ANY LEAKAGE WITHOUT SOFTWARE EFFORTS

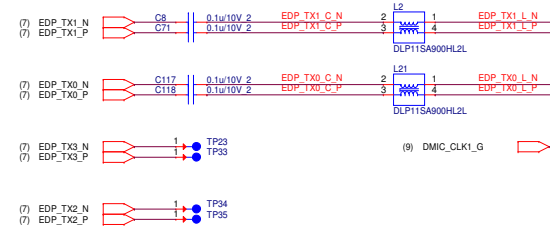
[illegible]

(21,22) MECH_PWR_BTN_IN_ODL

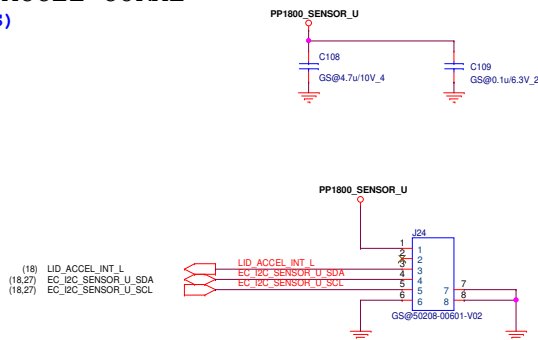
STUFF THESE FOR KEYBOARD POWER BUTTON

 Quanta Computer Inc. PROJECT : ZAK_ZAN_ZAP_ZAQ		
Size	Document Number KB, TP, PEN	Rev 1A
Date:	Tuesday, November 05, 2019	Sheet 25 of 45

EDP2-EDP3 DOES NOT NEED TO ROUTE TO CONNECTOR

[illegible]

(FCM)



(LDS)

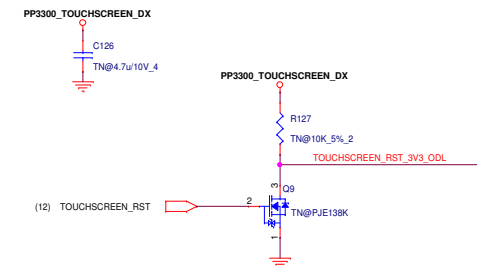


WFC CAMERA

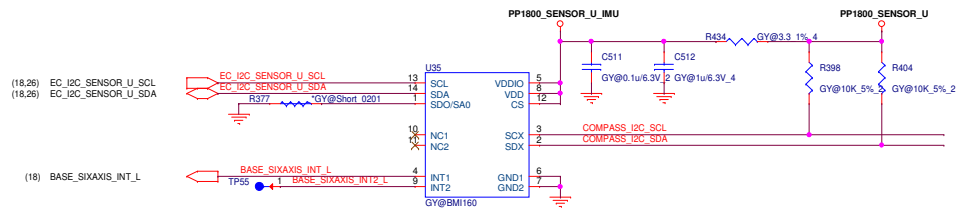
WFC INTERFACE PINOUT TBD. PENDING CHANGE



(TSN)



(GRS)



IMU

MODE 2 (SLAVE TO EC, MASTER TO MAG)
I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 7*0X68 (LSB SET BY SD0/SA0) -->8*0XD0H

(ACM)

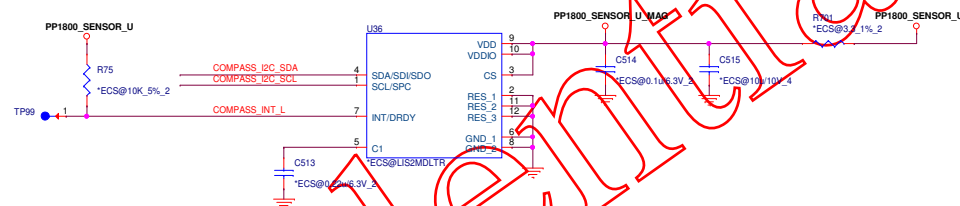
0 ohm for BOM option

R30Q~R32Q place near to IMU U35

EC I2C SENSOR U_SCL R30Q *ACM@0 5% 2
EC I2C SENSOR U_SDA R31Q *ACM@0 5% 2
BASE SIXAXIS_INT1_L R32Q *ACM@0 5% 2

for AR Camera, IMU can be DNS, but R30Q,R31Q,R32Q need to be stuffed

(ECS)

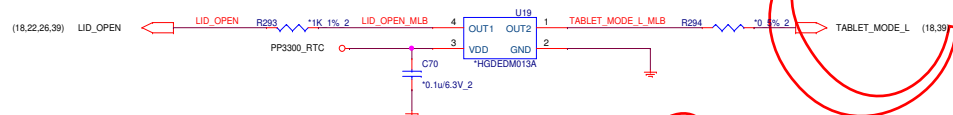


MAGNETOMETER

SLAVE TO IMU SENSOR
I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 0X1E

GMR SENSOR (RESERVED FOR ON BOARD SITUATION)

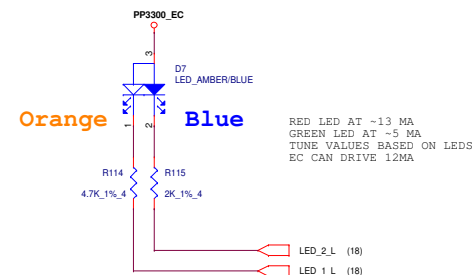
(GMR_MLB) For on board GMR



MAKE SURE TO CHECK THE POLARITY OF MAGNET TO ASSIGN THE PIN LID_OPEN AND TABLET-MODE
IF THE GMR SENSOR IS NOT PLACED ON THE MLB, PLEASE CAREFULLY PLAN THE PINOUT ON THE SUB-BOARD INTERFACE.

(UIF)

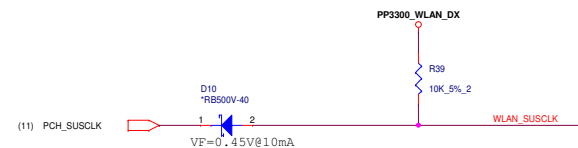
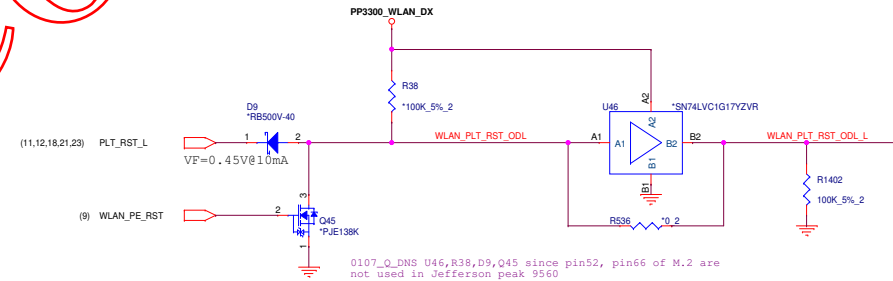
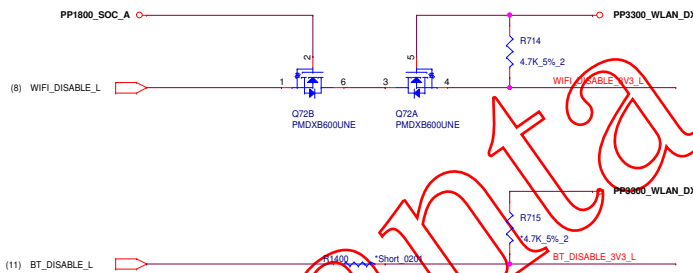
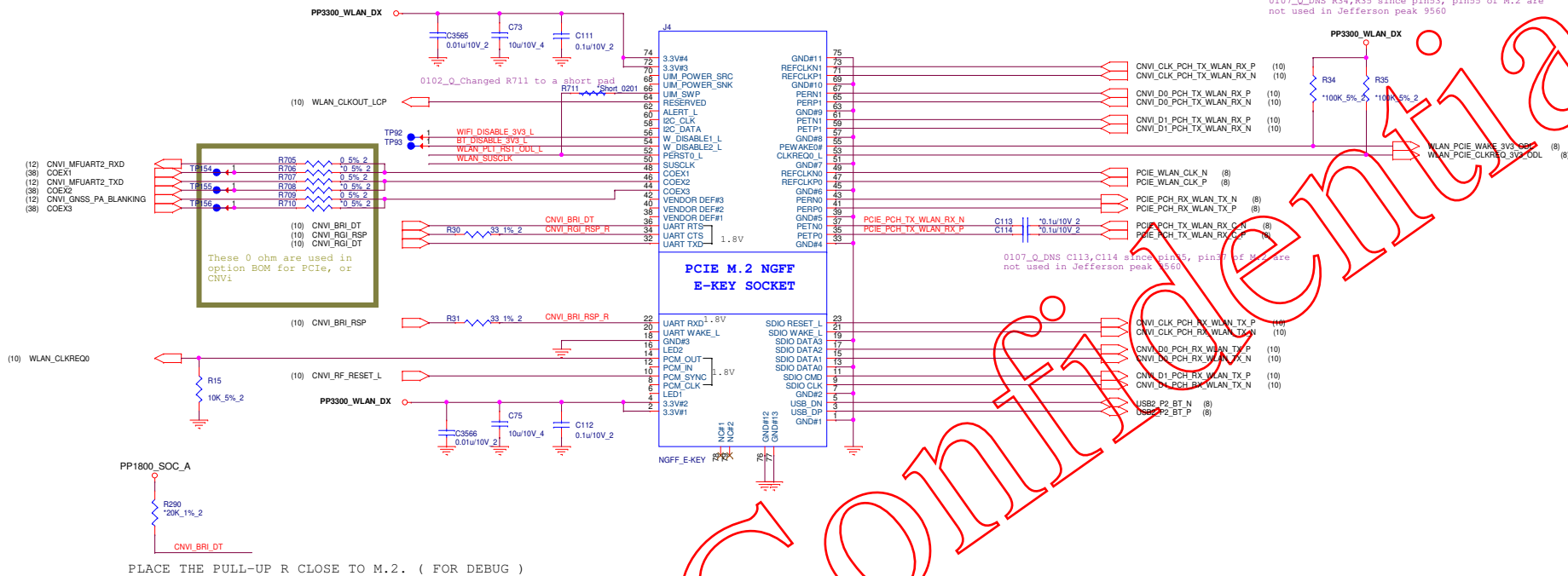
CHARGE/BATTERY LED



WIFI

CM TO CHOOSE CONNECTOR

(NGF)



U46,R38,D9,Q45,C113,C114,R34,R35,Q1,Q2 need to be stuffed for WiFi flexible design

(UTC1)

FOR USB-C PORT 0

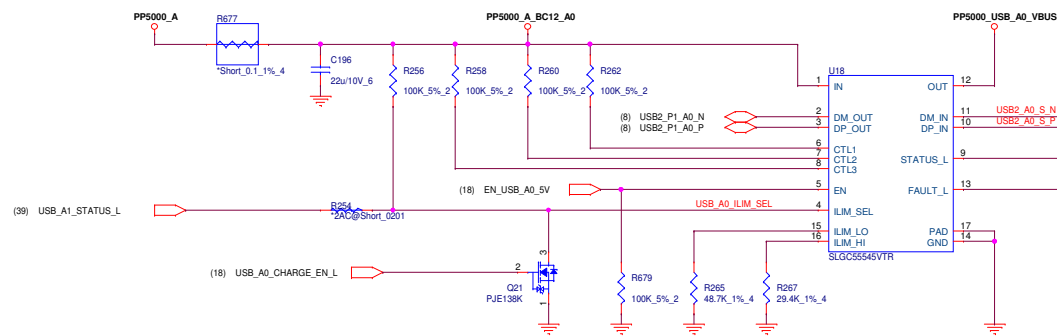
TO MLB CONNECTOR

leave USB_C0_DISCHARGE/EN_USB_C0_5V_3A_ILIM
NC and keep components being stuffed for
debug purpose

WITH THE NX20P3483, THE VBUS DISCHARGE CAN BE SW CONTROL

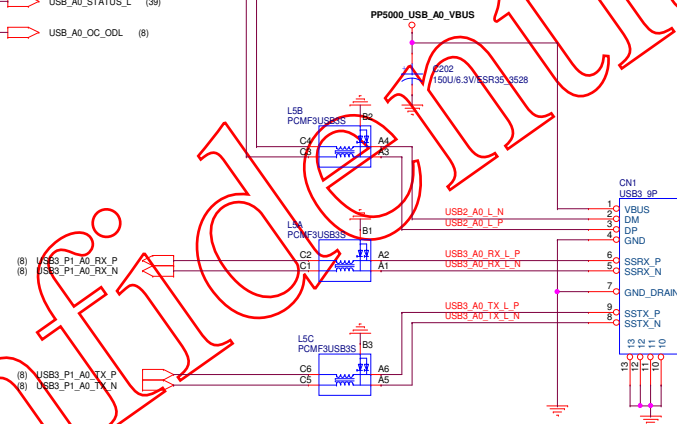
USB_C0_PD_RST IS ACTIVE HIGH WITH 100K INTERNAL PD

(UBC1)



(UB31)

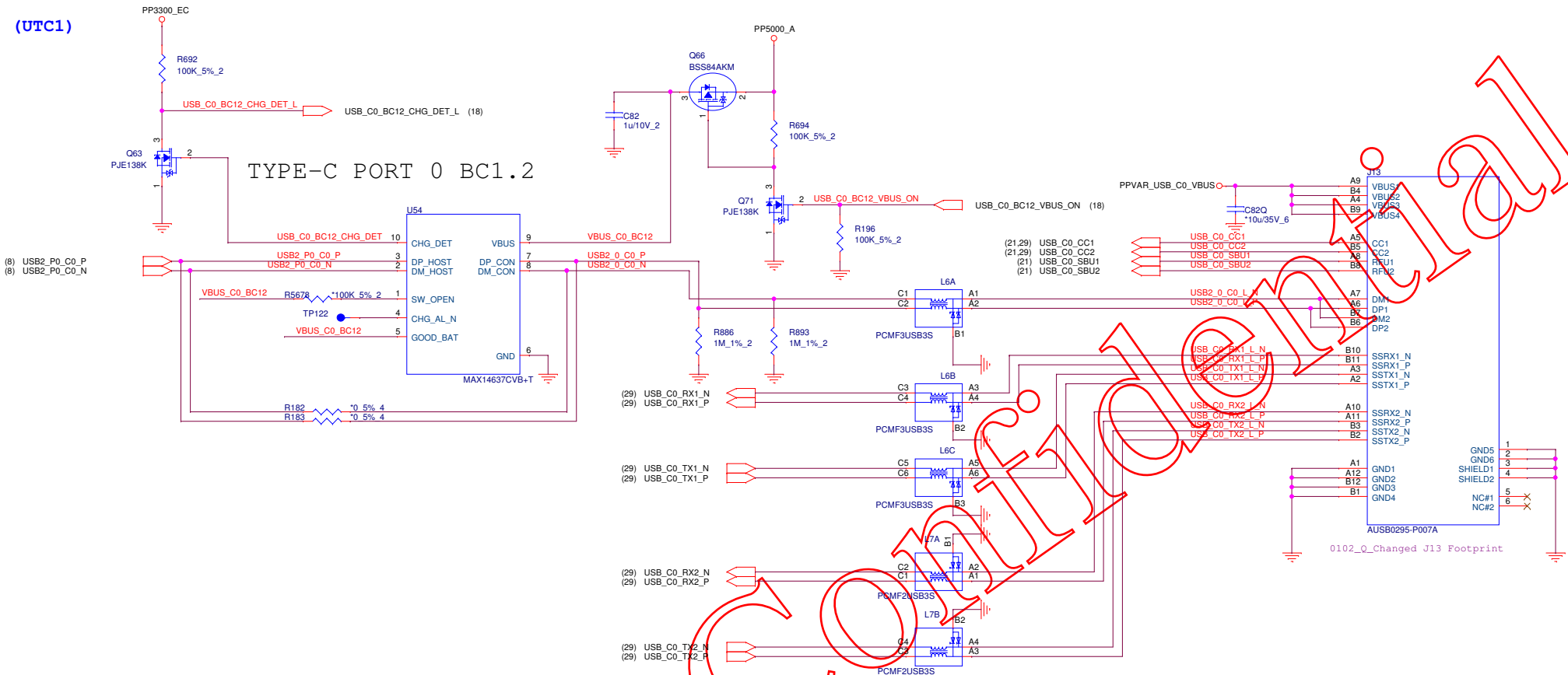
CM TO CHOOSE CONNECTOR



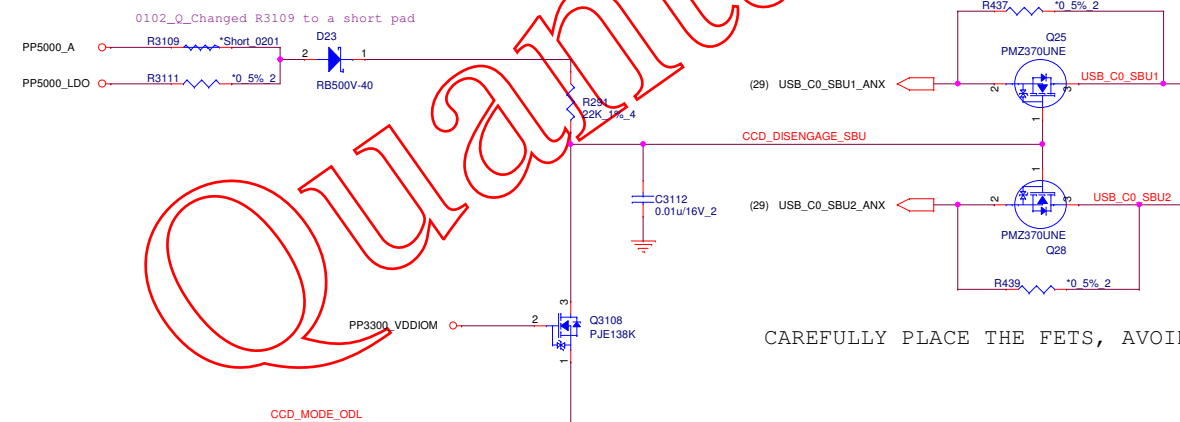
USB3.0 Type-A conn	11" ZBA/ZBB	1st	DFHS09FR780
		2nd	DFHS09FR790
	14" ZBC	1st	DFHS09FR937
		2nd	DFHS09FR936
	15" ZBD	1st	DFHS09FRB05
		2nd	DFHS09FRB06
3rd		DFHS09FRB07	

(UTC1)

TYPE-C PORT 0 BC1.2

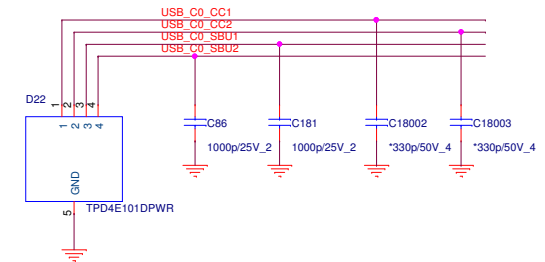


ONLY TIME CCD_DISENGAGE_SBU IS HIGH WHEN CCD_MODE IS INACTIVE AND THERE IS POWER TO THE TCPC



CAREFULLY PLACE THE FETS, AVOID LONG STUB

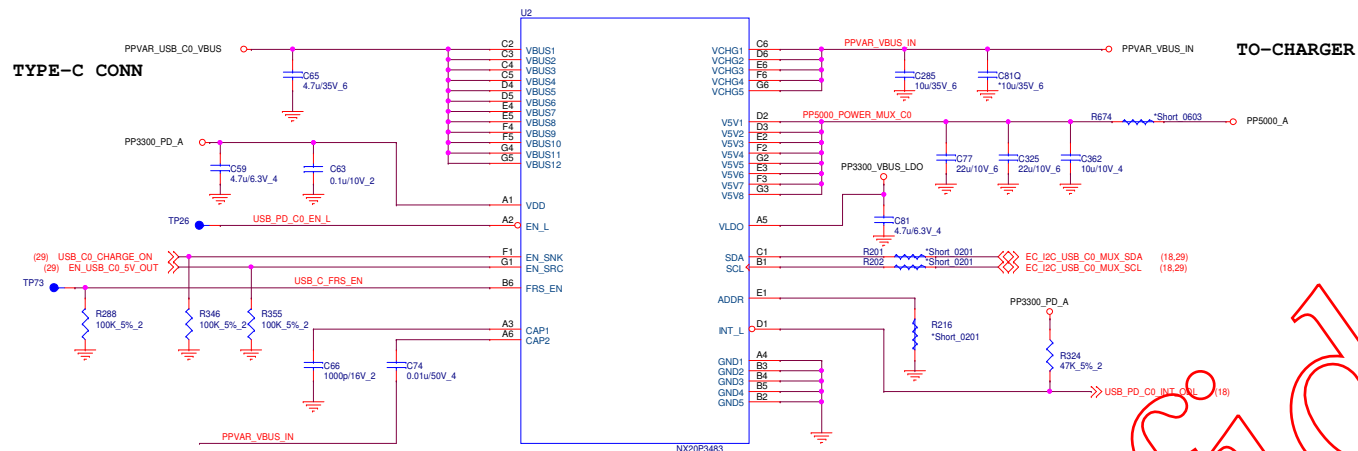
(UTC1)

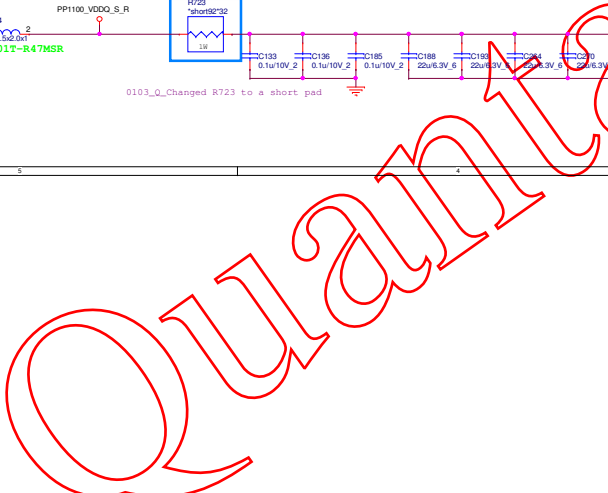


(PUB1)

PORT 0

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR

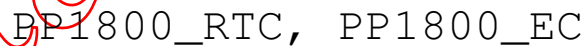




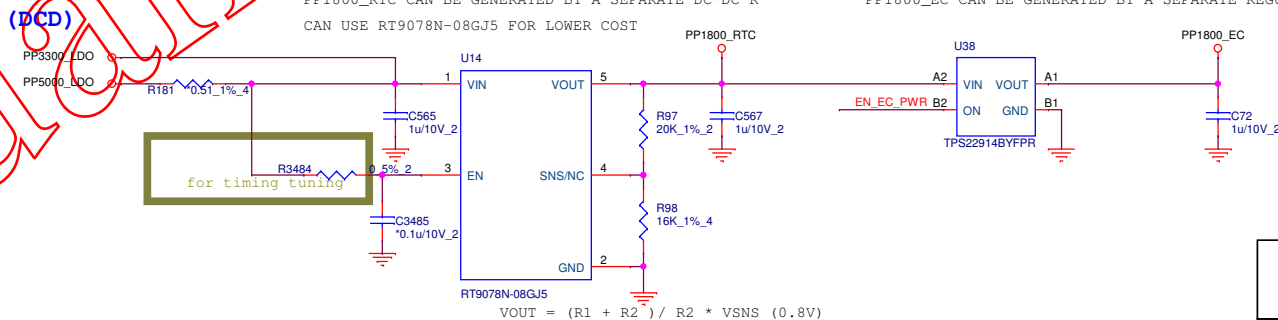
UVLO 4.5V- IF VBAT IS 2S, THEN WATCH OUT.



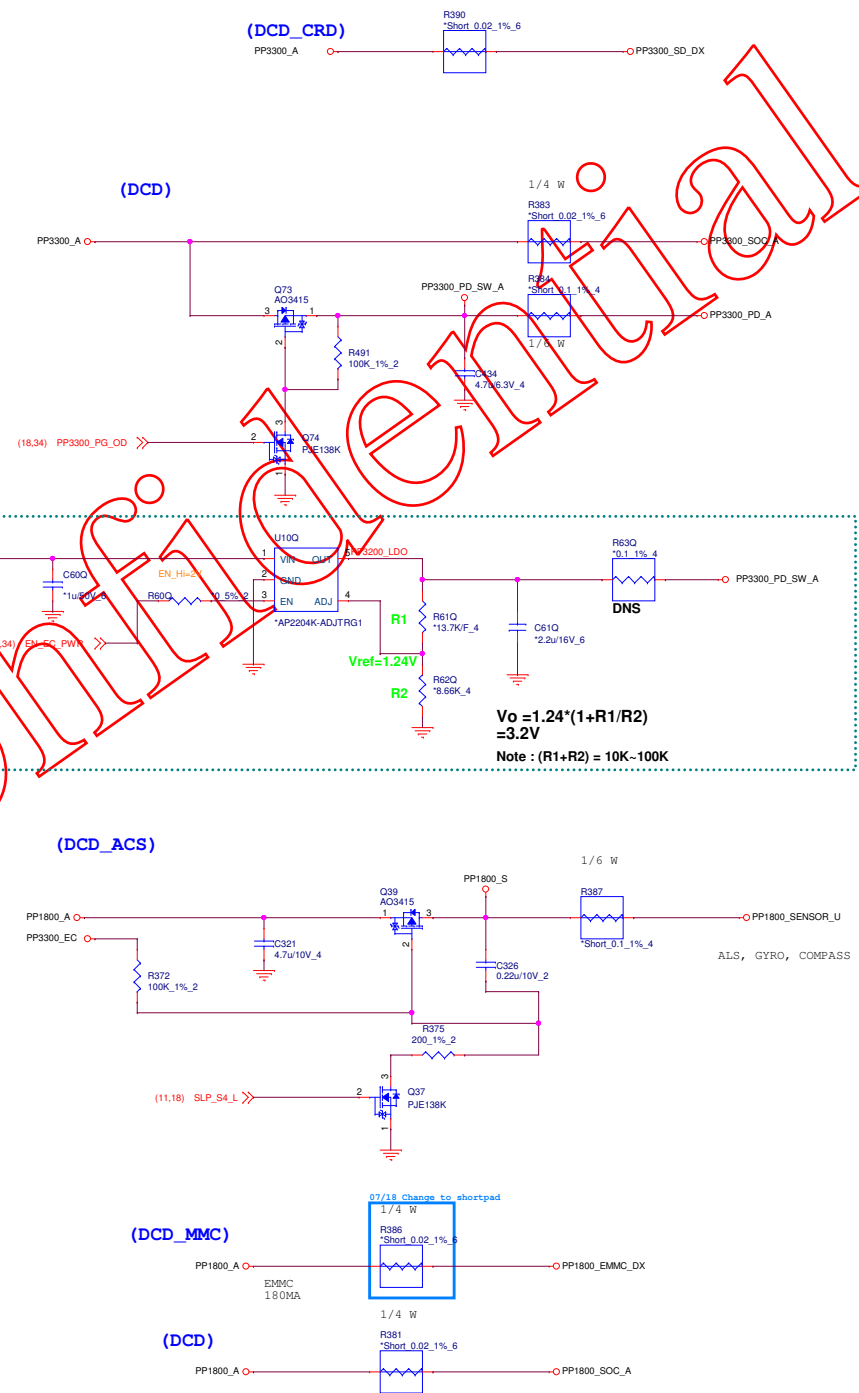
UVLO 5.4V - IF VBAT IS 2S, THEN WATCH OUT FOR VOLTAGE LOCK OUT FOR 1.8V



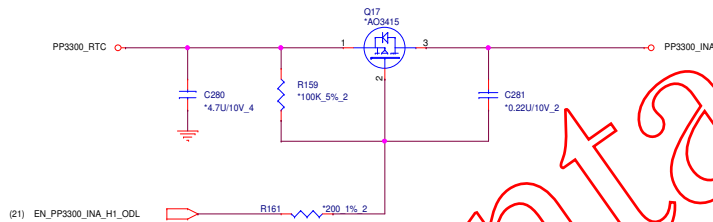
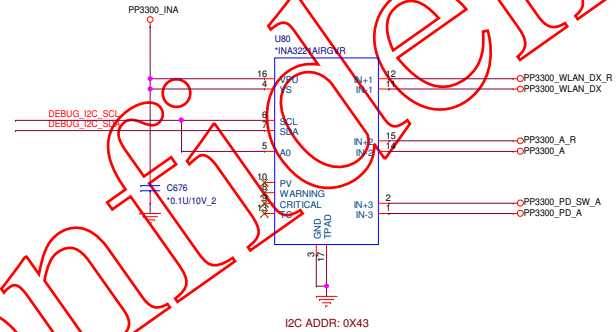
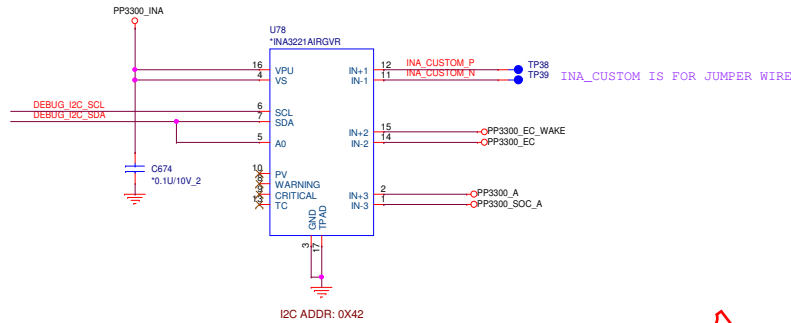
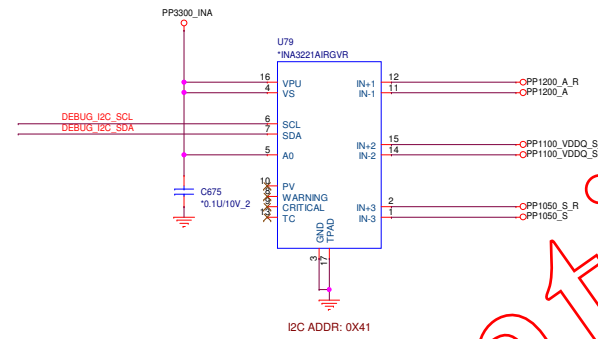
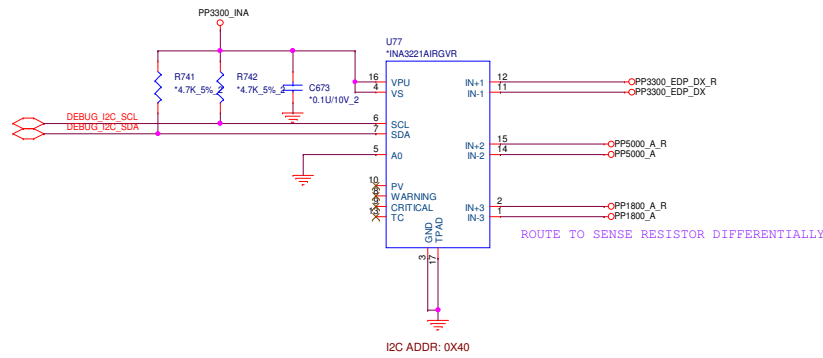
PP1800_EC CAN BE GENERATED BY A SEPARATE REGULATOR



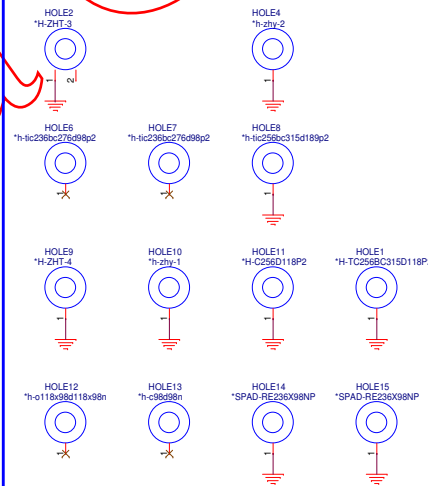
CHOICES FOR THE REGULATORS CAN BE SUBSTITUE AFTER CONFIRM THE FUNCTIONALITY.



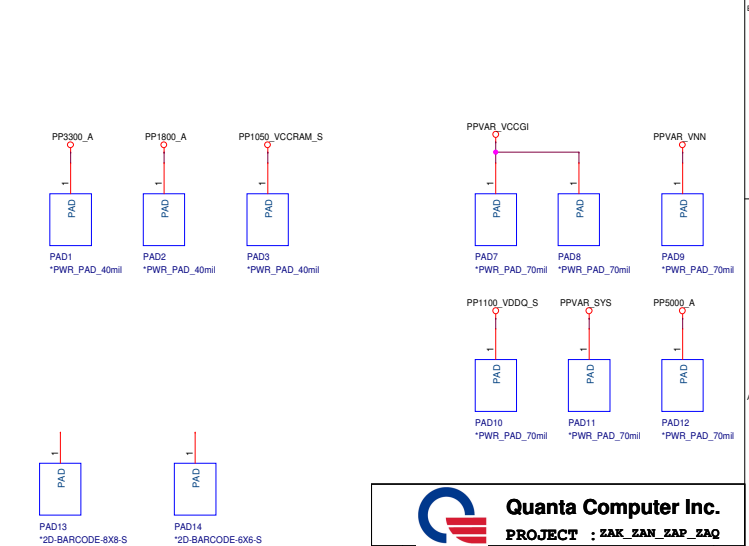
(INA)



HOLES (OTH)



POWER TEST PAD (OTH)



INTERSIL BUCK - BOOST CHARGER

INCREASE OR ADD POSCAPS IF AUDIBLE NOISE IS HEARD

RECOMMENDED VALUE
FROM DATASHEET

RECOMMENDED VALUE
FROM DATASHEET

REQUIRE HIGHER
OUTPUT CAPACITANCE

RATING
HIGH ENOUGH?

0102_Q_removed R475,R476,R477,R478 used as 0-ohm jumper
EVT/DVT builds for layout optimization

ADAPTER VOLTAGE
VALID IF > 3.4V

PULL-UP FROM EC OR H1?

C541 GND PIN SHOULD GOES TO PIN E1 AVSS OF U45

I2C ADDR : 0X12

FOR 0.476A ADAPTER CURRENT LIMIT
AND 733KHz SWITCHING FREQUENCY:
2CELL : 93.1K
3CELL : 105K

0102_Q_Changed R424 to a short pad

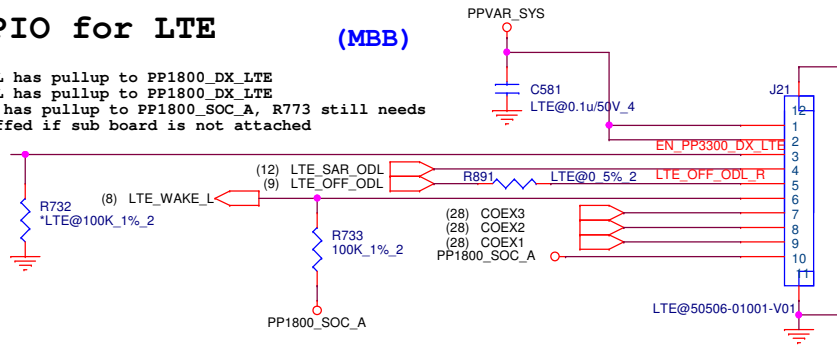
CV: 12.6V
3S1P Battery

GPIO for LTE

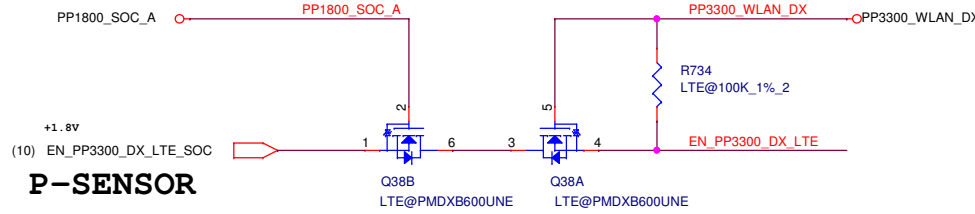
(MBB)

Coral sub board

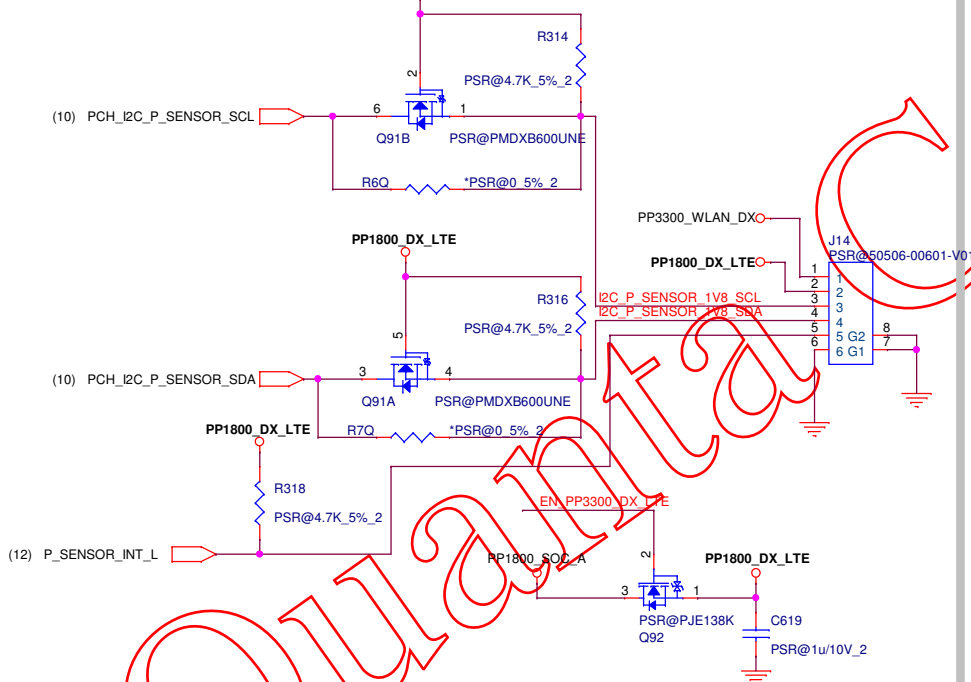
- LTE_SAR_ODL has pullup to PP1800_DX_LTE
- LTE_OFF_ODL has pullup to PP1800_DX_LTE
- LTE_WAKE_L has pullup to PP1800_SOC_A, R773 still needs to be stuffed if sub board is not attached



LEVERAGING CORAL BOARD!



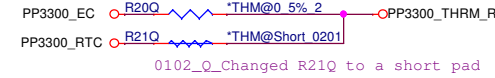
(PXS)



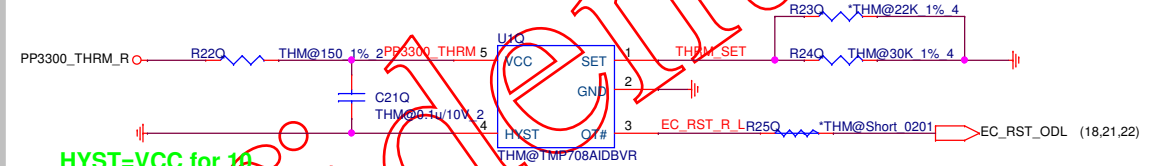
(SYS_THM)

Thermal Protector

Need fine tune
for thermal protect point
Note placement position
TEMP=76.3C



$$R_{set}(Kohm) = 0.0012T^*T - 0.9308T + 96.147$$



HYST=VCC for 10
degree Hys.
HYST=GND for 30
degree Hys.

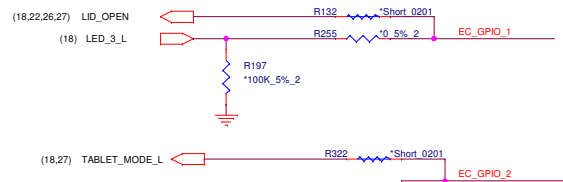


Quanta Computer Inc.

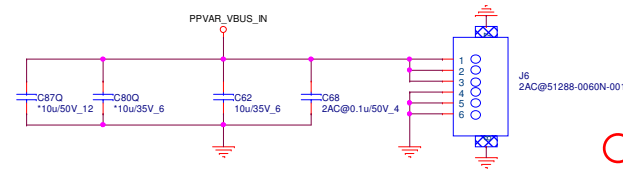
PROJECT : ZAK_ZAN_ZAP_ZAQ

Size	Document Number	Rev
	LTE\$TEST	1A
Date:	Tuesday, November 05, 2019	Sheet 38 of 45

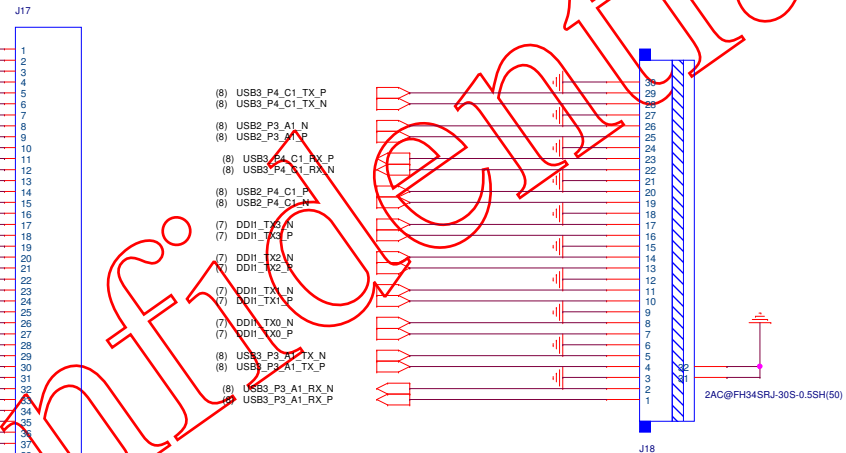
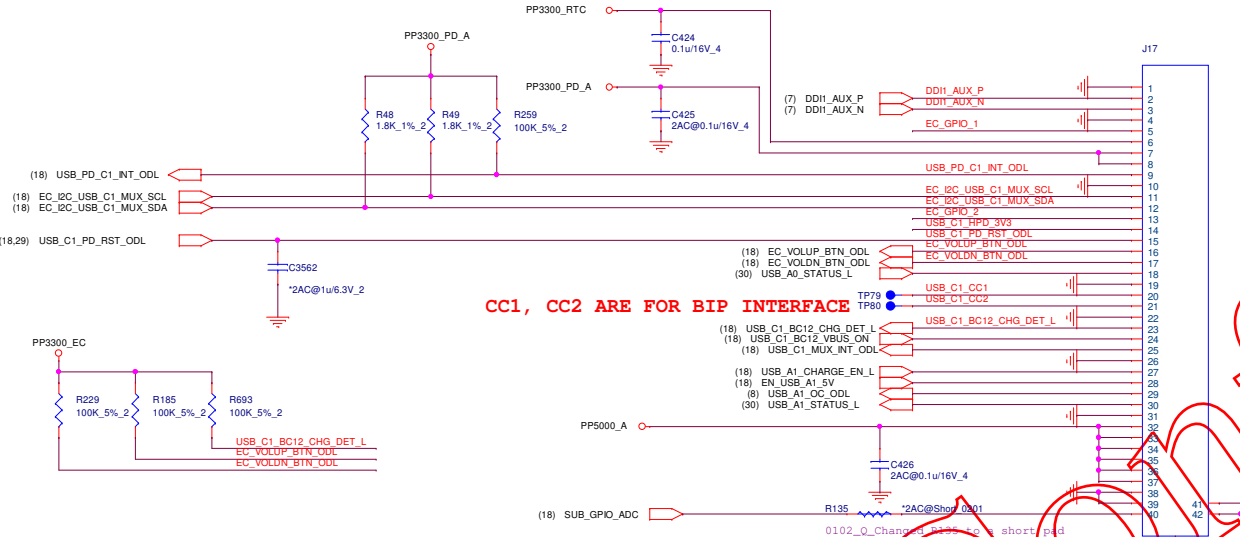
(UTC2)



EC_GPIO1,2 CAN BE USED FOR CONNECTING THE GMR SENSOR ON THE SUB-BOARD
OR IT CAN BE USED TO CONNECT AN SPARE EC GPIO PINS FOR ADDITIONAL CONTROL FROM EC

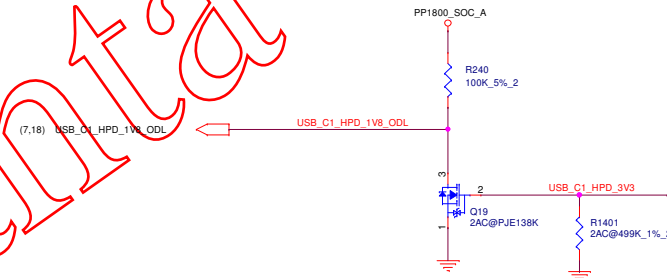


PULL-DOWN RESISTORS TO AVOID
FLOATING INPUT W/O SUB-BOARD



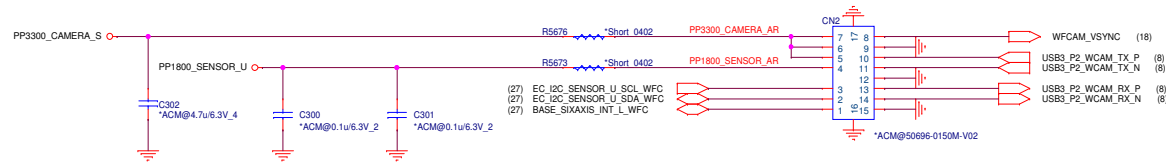
SELECT PER SEL SI TEAM

SELECT PER SEL SI TEAM
CM TO ADJUST PINOUT/PIN COUNT

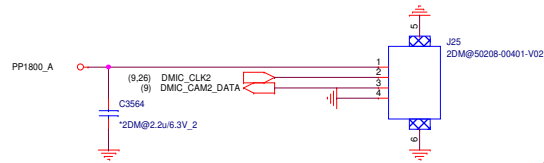


MOTHER BOARD INTERFACE

AR CAMERA CONN (ACM)



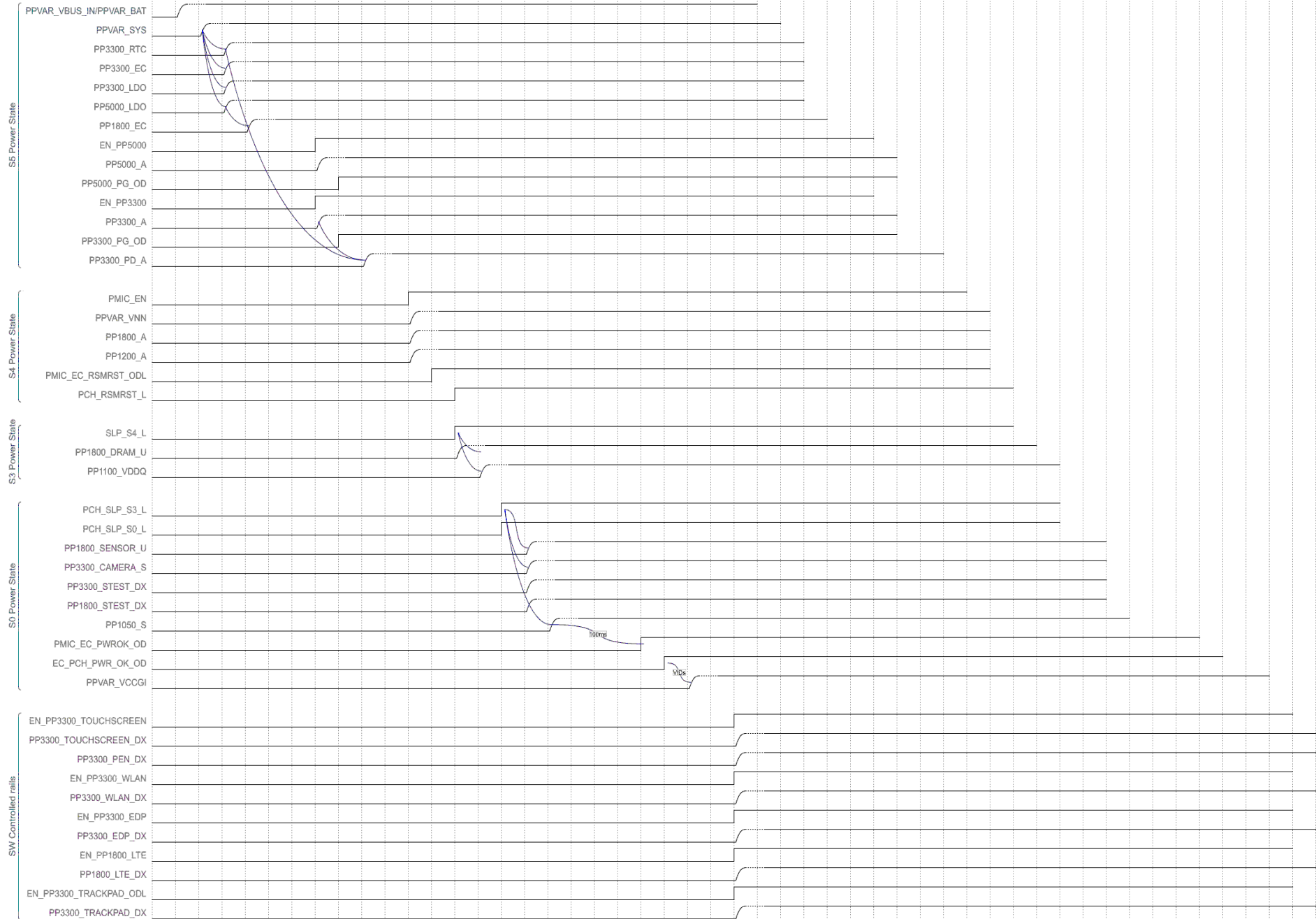
DMIC CONN (MIC2)



PREFERRED DMIC CHANNEL CONFIG
INTERFACE 1: STRAP MIC TO LEFT=CHANNEL 0
INTERFACE 2: STRAP MIC TO RIGHT=CHANNEL 3

Quanta Confidential

Quanta Confidential



GPIO #	Bump Name	Voltage	Bootstrap Termination	Default Termination	Bootstrap Purpose	Bootstrap Usage	Bootstrap	Octopus Signal Name
GPIO_27	GPIO_27	1.8V	20K PU	20K PD	eMMC as boot Source 20K PU internal	1 = enable (default) 0 = disable	eMMC Boot	DBG_PTI_DATA_16
GPIO_28	GPIO_28	1.8V	20K PU	20K PD	SPI as boot Source 20K PU internal	1 = enable (default) 0 = disable	SPI Boot	DBG_PTI_DATA_17
GPIO_42	GP_INTD_DS1_TE1	1.8V	20K PD	20K PD	Flash Descriptor Override for SPI security features	1 = Override 0 = No Override (default)	Flash Descriptor	TP_WIFI_RST_N, TP135
GPIO_43	GP_INTD_DS1_TE2	1.8V	20K PU	20K PD	RSVD	1 = Disable (default) 0 = Do Not Use	RSVD	GP_INTD_DS1_TE2
GPIO_44	USB_OC0_B	1.8V	20K PD	20K PU	RVSD	1 = Do Not Use 0 = disable (default)	RSVD	USB_A_OC_ODL
GPIO_45	USB_OC1_B	1.8V	20K PD	20K PU	Top Swap Override. Have core look for BIOS code in SPI ROM	1 = Enable 0 = disable (default)	Top Swap	USB_C_OC_ODL
GPIO_61	LPSS_UART0_TXD	1.8V	20K PD	20K PU	TXE to bypass ROM in SoC and go to patch space	1 = enable bypass 0 = disable (default)	TXE ROM Bypass	PCHTX_MIP160RX_UART
GPIO_62	LPSS_UART0_RTS	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = disable (default)	RSVD	stest_INT_L
GPIO_65	LPSS_UART2_TXD	1.8V	20K PD	20K PU	TXE to perform DnX for new FW Image over USB.	1 = Force DnX 0 = Do Not Force (default)	DnX FW Load	PCHTX_UART2
GPIO_66	LPSS_UART2_RTS	1.8V	20K PD	20K PU	LPC Boot BIOS strap	1 = LPC Boot 0 = No LPC Boot (default)	LPC Boot	LTE_OFF_ODL
GPIO_79	LPSS_SPI_0_CLK	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	H1_SLAVE_SPI_CLK_R
GPIO_80	LPSS_SPI_0_FSD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = No halt (default)	RSVD	H1_SLAVE_SPI_CS_L_R
GPIO_81	LPSS_SPI_0_FS1	1.8V	20K PU	20K PU	RSVD	1 = Disable (default) 0 = Do Not Use	RSVD	GPIO_81_DEBUG (Boot halt)
GPIO_83	LPSS_SPI_0_TXD	1.8V	20K PD	20K PD	Sets the LPC buffer to 1.8V or 3.3V mode	1 = 1.8V mode 0 = 3.3V mode (default)	LPC Voltage Select	H1_SLAVE_SPI_MOSI_R
GPIO_84	LPSS_SPI_2_CLK	1.8V	20K PU	20K PD	SPI Boot BIOS Strap	1 = Don't SPI Boot (default) 0 = SPI Boot Debug if Secure boot fuse is set to 0	SPI Boot Source	stest_SPI1_CLK_R
GPIO_85	LPSS_SPI_2_FSD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = disable (default)	RSVD	stest_SPI_CS_L_R
GPIO_86	LPSS_SPI_2_FS1	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = enable (default)	RSVD	stest_CNTRL
GPIO_87	LPSS_SPI_2_FS2	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	TP_PCH_GPIO_87_PD
GPIO_89	LPSS_SPI_2_TXD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	stest_SPI1_MOSI_R
GPIO_159	AVS_I2S0_SDI	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	I2S0_PCH_RX
GPIO_163	AVS_I2S1_WS_SYN	1.8V	20K PD	20K PD	SMBus 3.3V/1.8V mode select	1 = 1.8V mode 0 = 3.3V mode (default)	Buffers 1.8V/3.3V	I2S_SFRM_5PKR
GPIO_164	AVS_I2S1_SDI	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	WLAN_PE_RST
GPIO_168	AVS_HDA_SDI	1.8V	20K PD	20K PD	PMU 3.3V/1.8V mode select	1 = 1.8V mode 0 = 3.3V mode (default)	PMU 1.8V/3.3V	I2S2_PCH_RX
GPIO_172	AVS_M_CLK_B1	1.8V	20K PD	20K PD	SMBus No Reboot. Handled by PMC	1 = Enable 0 = disable (default)	SMBus Reboot	DMIC_CLK2_R
GPIO_174	AVS_M_CLK_AB2	1.8V	20K PD	20K PD	VDD2 Voltage Select	1 = 1.24V 0 = 1.20V (default)	VDD2 Voltage	(Open, TP_GPIO_174)
GPIO_175	AVS_M_DATA_2	1.8V	20K PD	20K PD	eSPI vs. LPC	1 = eSPI mode 0 = LPC mode (default)	eSPI/LPC mode	DMIC_CAM2_DATA
GPIO_177	SMB_CLK	1.8V/3.3V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	(Open, TP160)
GPIO_191	CNV_BRI_DT	1.8V	20K PD	None	eSPI Flash Sharing Mode. Set to 0 if GPIO_175 is set to 0	1 = Slave attached Share 0 = Master attached (default)	Flash Sharing	CNVI_BRI_DT_R
GPIO_192	CNV_BRI_RSP	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_BRI_RSP
GPIO_193	CNV_RGI_DT	1.8V	20K PU	None	RSVD	1 = Normal Operation 0 = Do not use	RSVD	CNVI_RGI_DT_R
GPIO_194	CNV_RGI_RSP	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_RGI_RSP
GPIO_195	CNV_RF_RESET_B	1.8V	20K PD	None	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_RF_RESET_L
GPIO_196	XTAL_CLKREQ	1.8V	20K PD	None	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	(Not available)